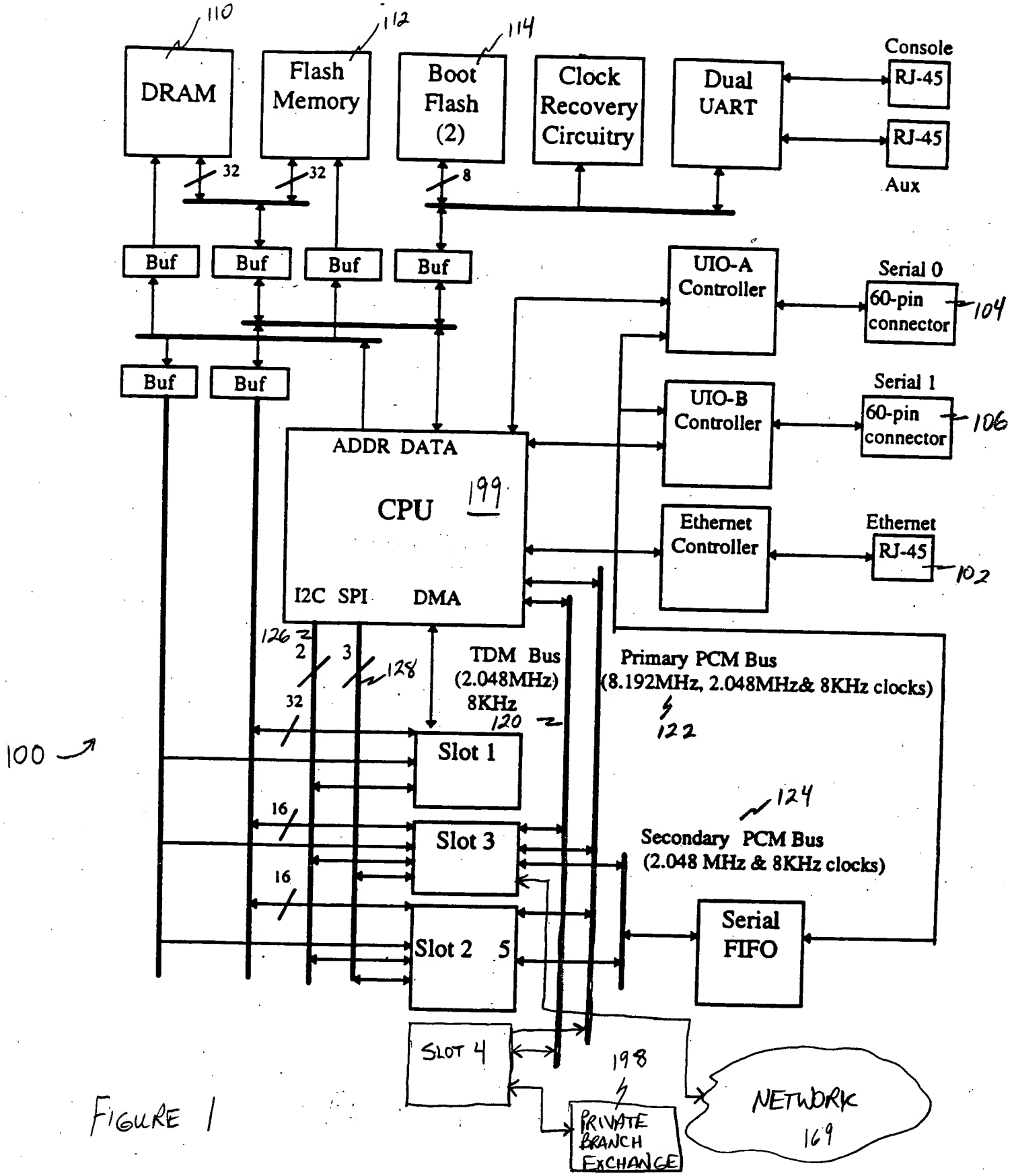

110
112
114
DRAM
Flash Memory
Boot Flash (2)
Clock Recovery Circuitry
Dual UART
Console
RJ-45
RJ-45
Aux
32
32
8
Buf
Buf
Buf
Buf
Buf
Buf
UIO-A Controller
Serial 0
60-pin connector
104
UIO-B Controller
Serial 1
60-pin connector
106
ADDR DATA
CPU
199
I2C SPI DMA
Ethernet Controller
Ethernet
RJ-45
102
126
2
3
128
TDM Bus (2.048MHz) 8KHz
120
Primary PCM Bus (8.192MHz, 2.048MHz& 8KHz clocks)
122
32
Slot 1
124
16
Slot 3
Secondary PCM Bus (2.048 MHz & 8KHz clocks)
16
Slot 2
5
Serial FIFO
SLOT 4
198
PRIVATE BRANCH EXCHANGE
NETWORK
169
100

FIGURE 1

860E60" 92hh9T60

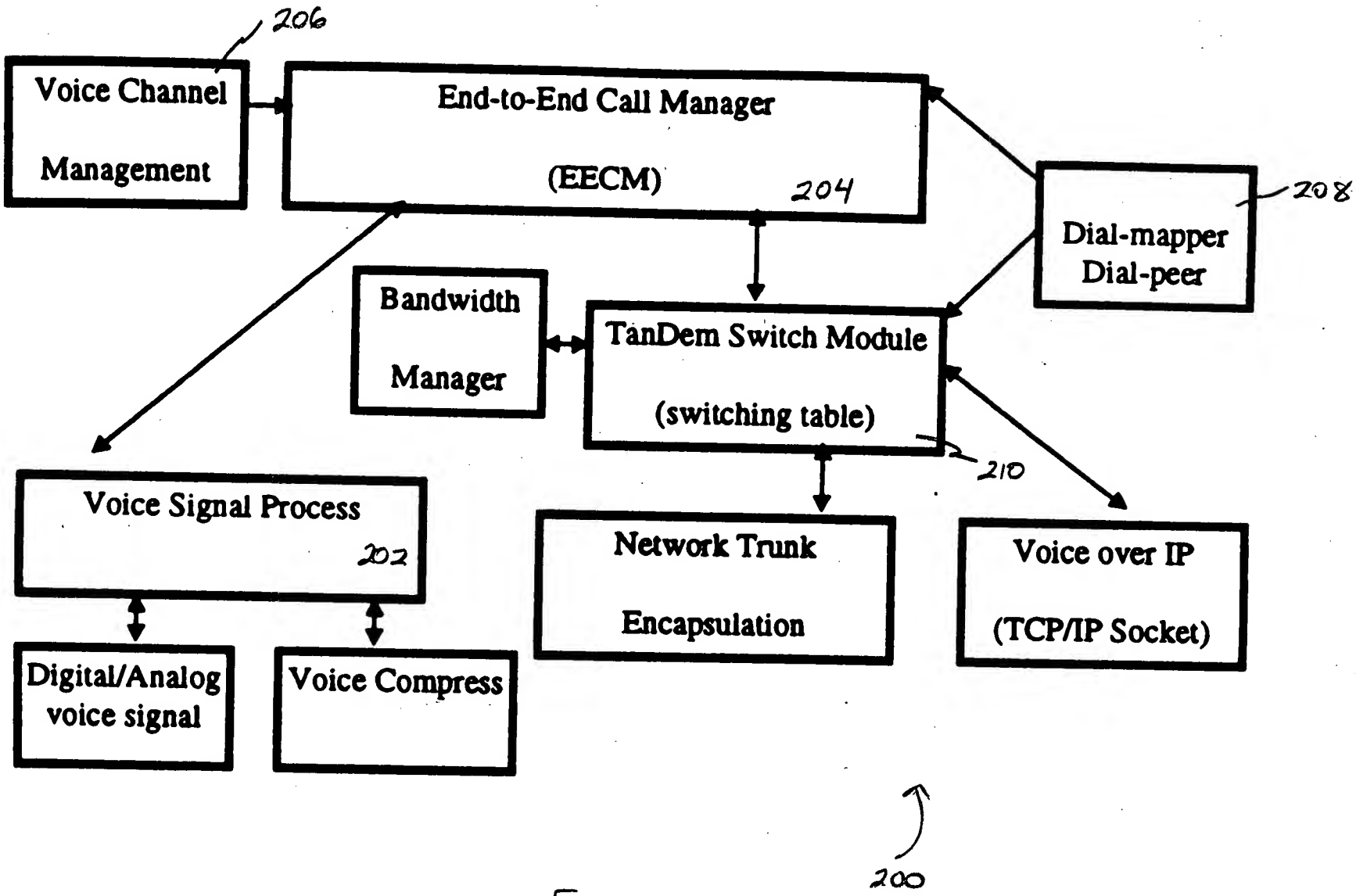


FIGURE 2

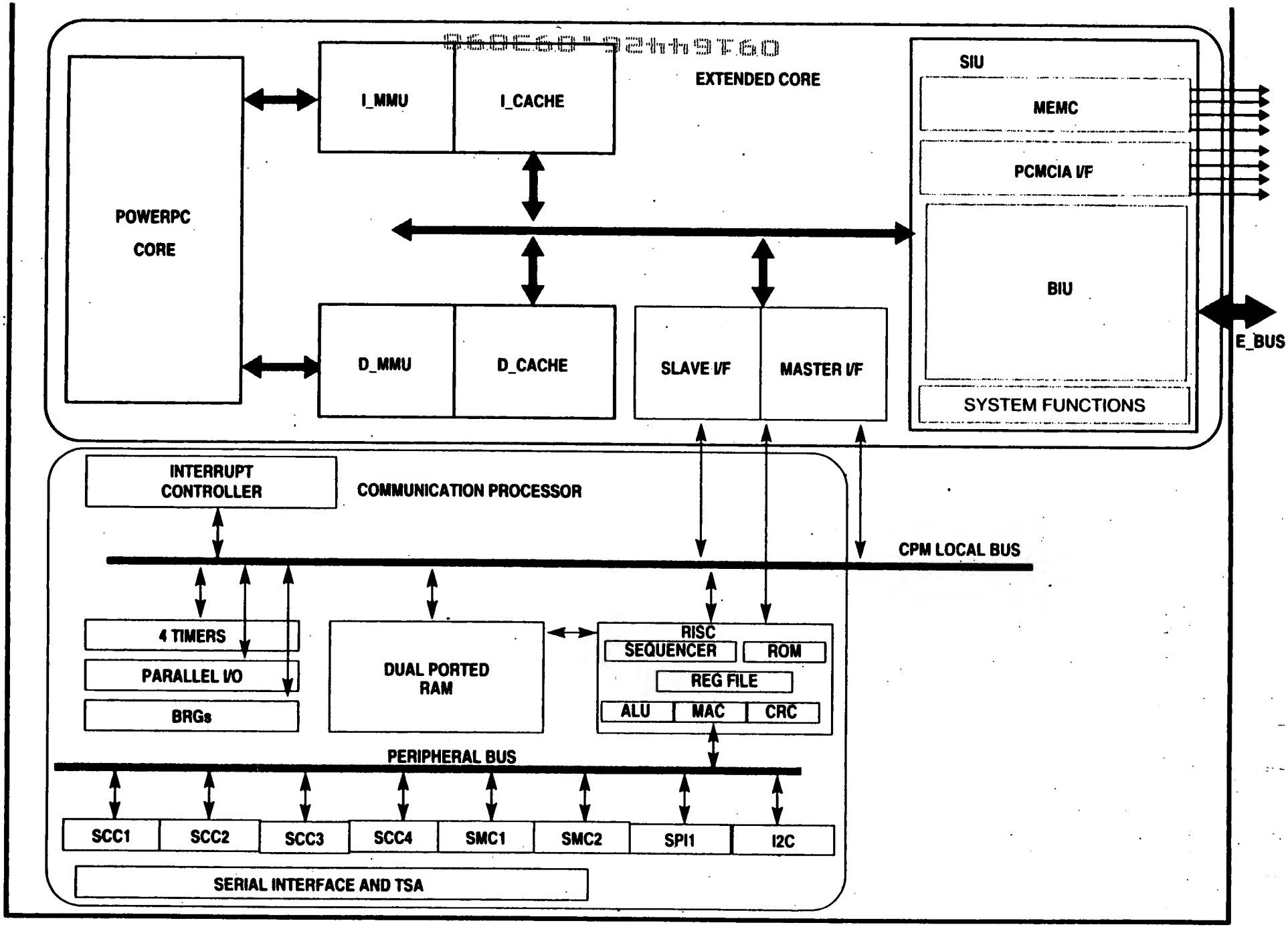

MPC860 PowerQUICC
EXTENDED CORE
POWERPC
CORE
I_MMU
I_CACHE
D_MMU
D_CACHE
SLAVE I/F
MASTER I/F
SIU
MEMC
PCMCIA I/F
BIU
SYSTEM FUNCTIONS
E_BUS
INTERRUPT
CONTROLLER
COMMUNICATION PROCESSOR
CPM LOCAL BUS
4 TIMERS
PARALLEL I/O
BRGs
DUAL PORTED
RAM
RISC
SEQUENCER
ROM
REG FILE
ALU
MAC
CRC
PERIPHERAL BUS
SCC1
SCC2
SCC3
SCC4
SMC1
SMC2
SPI1
I2C
SERIAL INTERFACE AND TSA

FIGURE 3

860660 "92h9T60

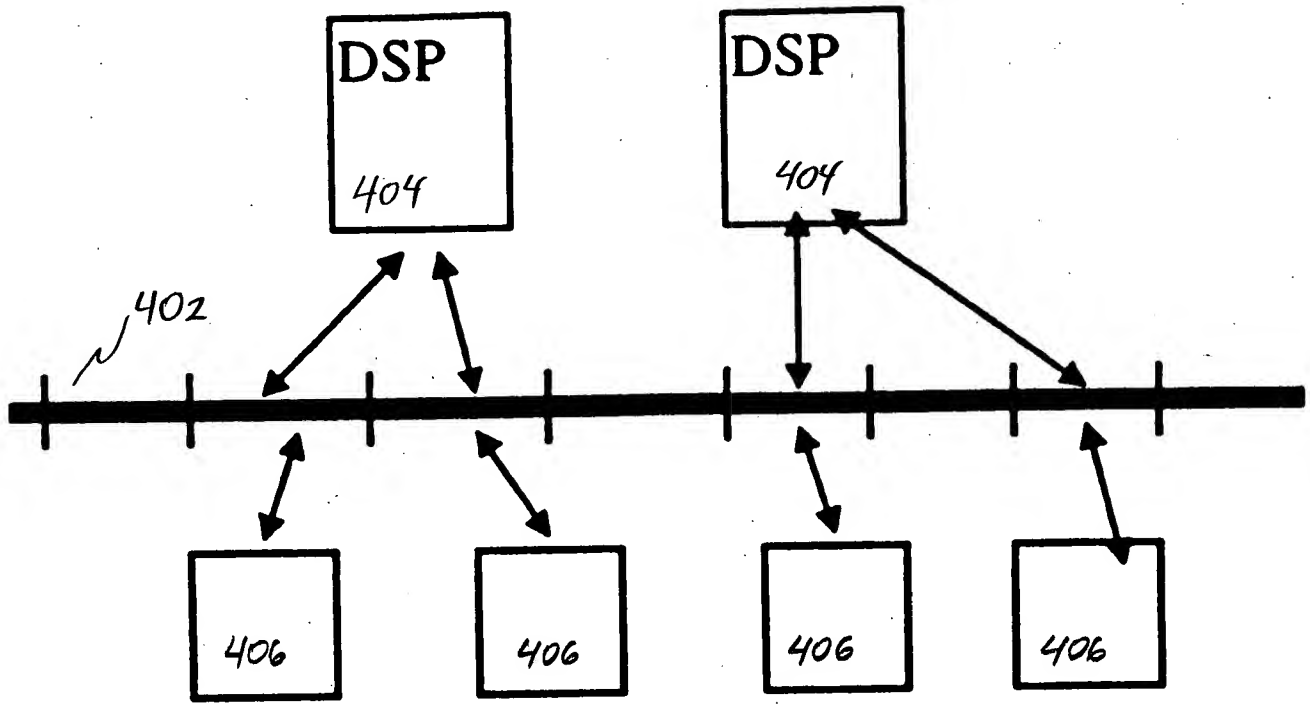


FIGURE 4

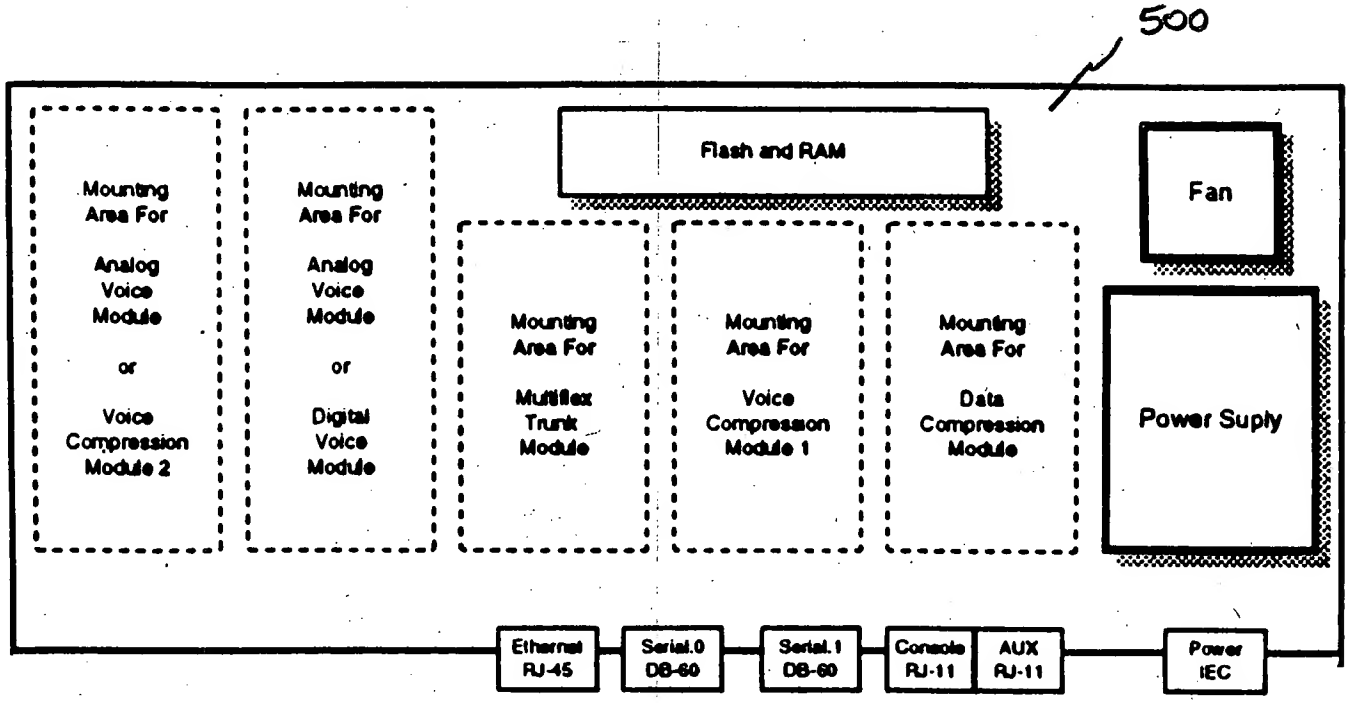

500
Mounting Area For Analog Voice Module or Voice Compression Module 2
Mounting Area For Analog Voice Module or Digital Voice Module
Flash and RAM
Mounting Area For Multiflex Trunk Module
Mounting Area For Voice Compression Module 1
Mounting Area For Data Compression Module
Fan
Power Suply
Ethernet RJ-45
Serial.0 DB-60
Serial.1 DB-60
Console RJ-11
AUX RJ-11
Power IEC

FIGURE 5

860660 92hh9760

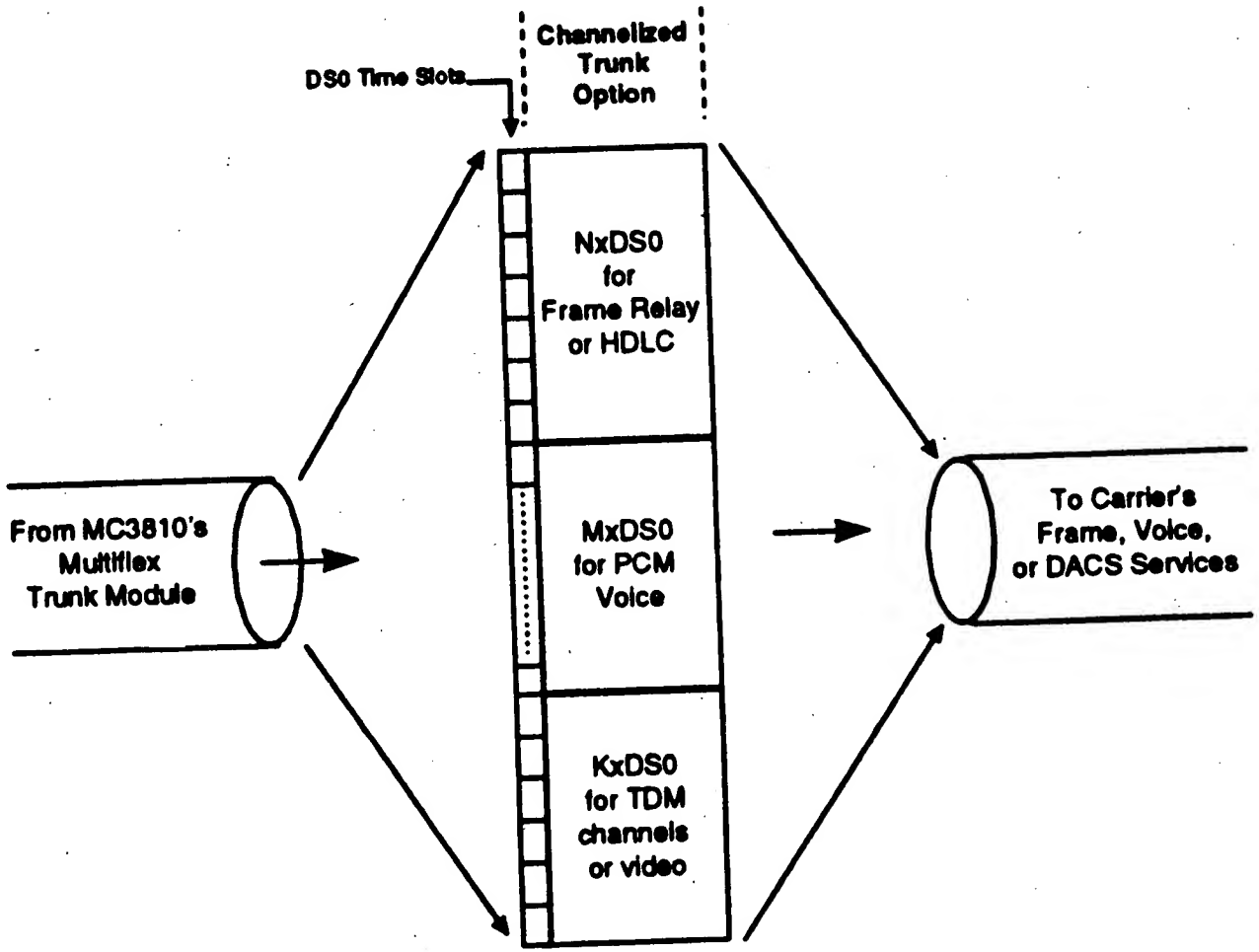


FIGURE 6

860660 " 92th9T60

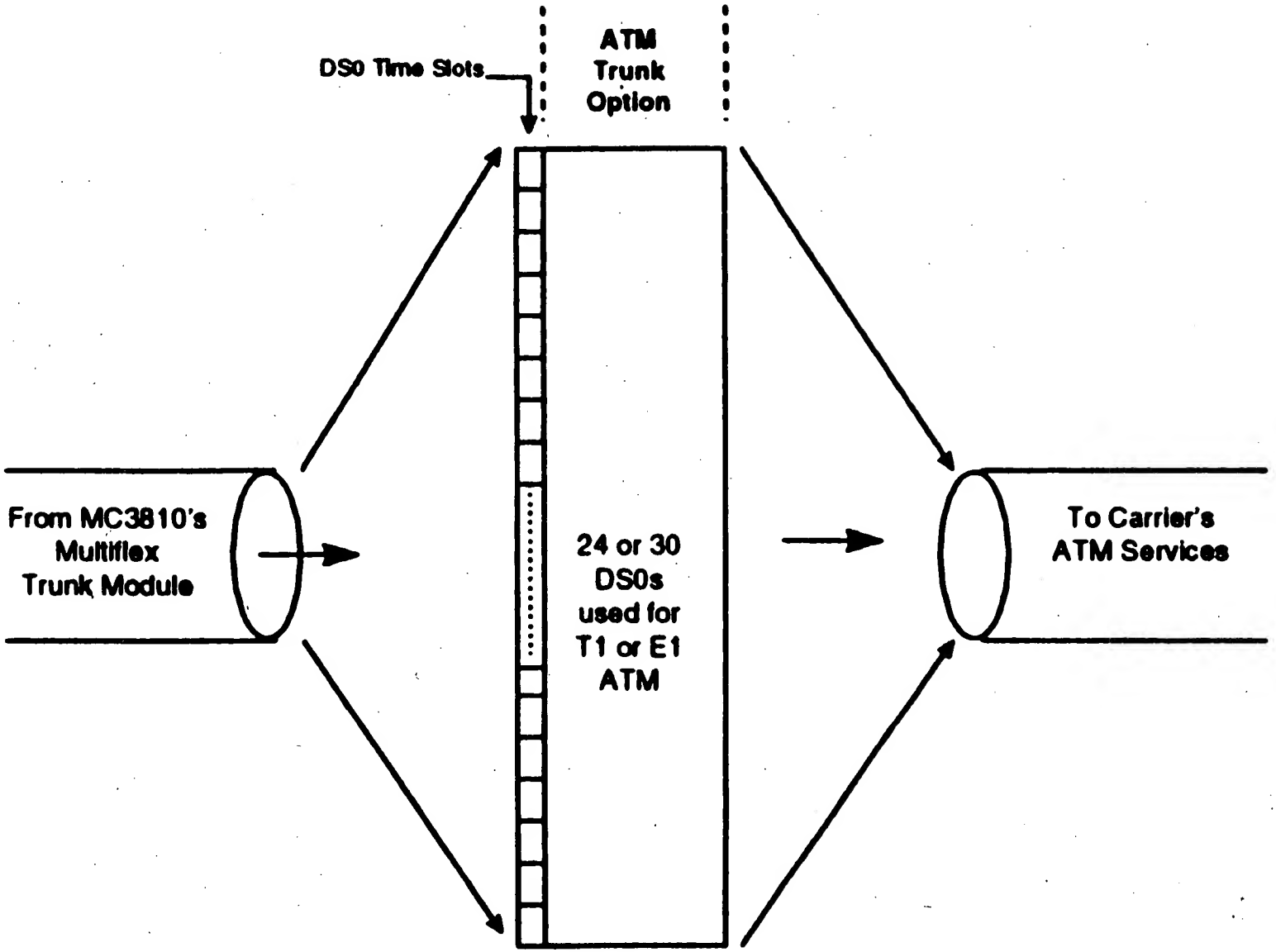


FIGURE 7

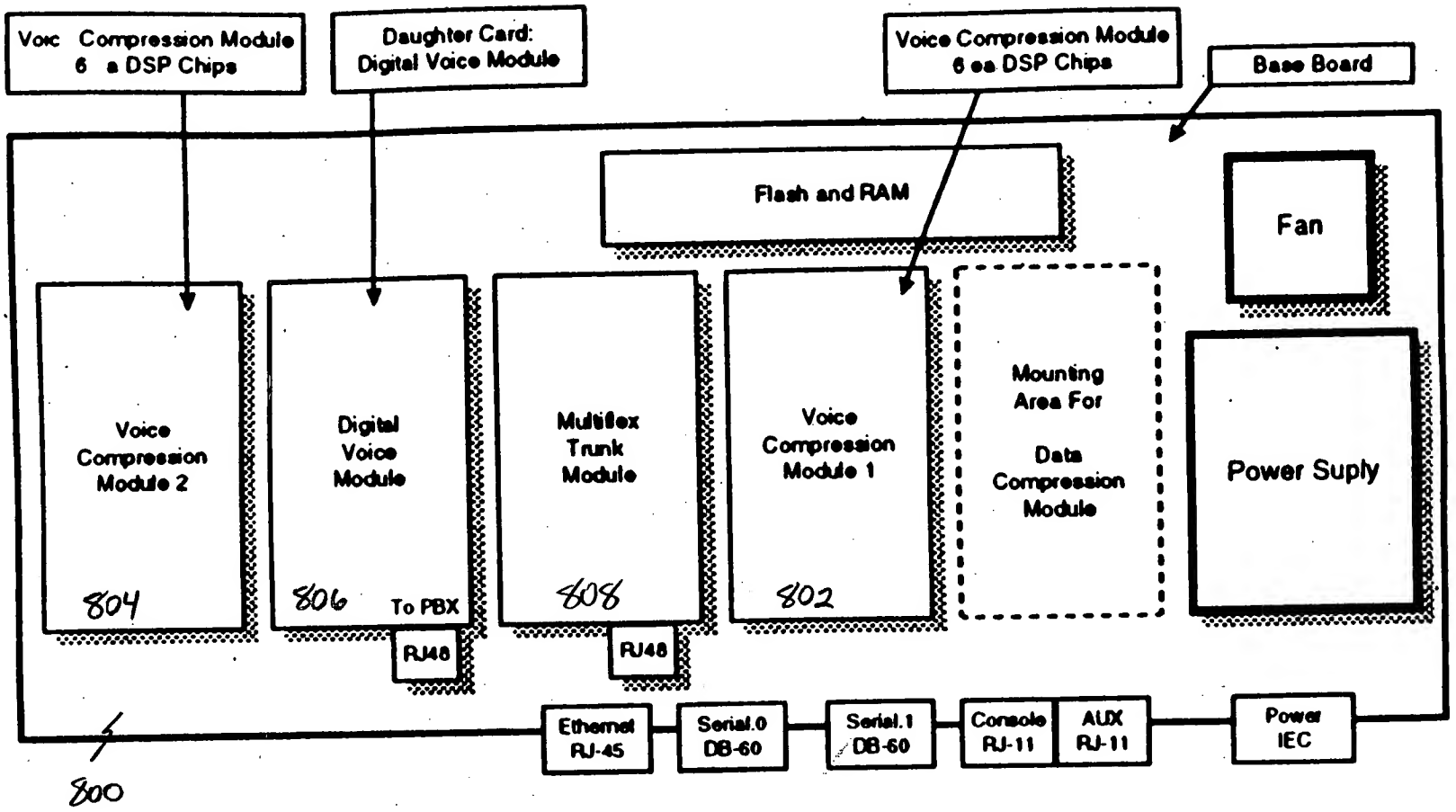

Voice Compression Module
6 ea DSP Chips
Daughter Card:
Digital Voice Module
Voice Compression Module
6 ea DSP Chips
Base Board
Flash and RAM
Fan
Voice
Compression
Module 2
804
Digital
Voice
Module
806
To PBX
RJ48
Multiflex
Trunk
Module
808
RJ48
Voice
Compression
Module 1
802
Mounting
Area For
Data
Compression
Module
Power Suply
Ethernet
RJ-45
Serial.0
DB-60
Serial.1
DB-60
Console
RJ-11
AUX
RJ-11
Power
IEC
800

FIGURE 8

860E60" 92hh9T60

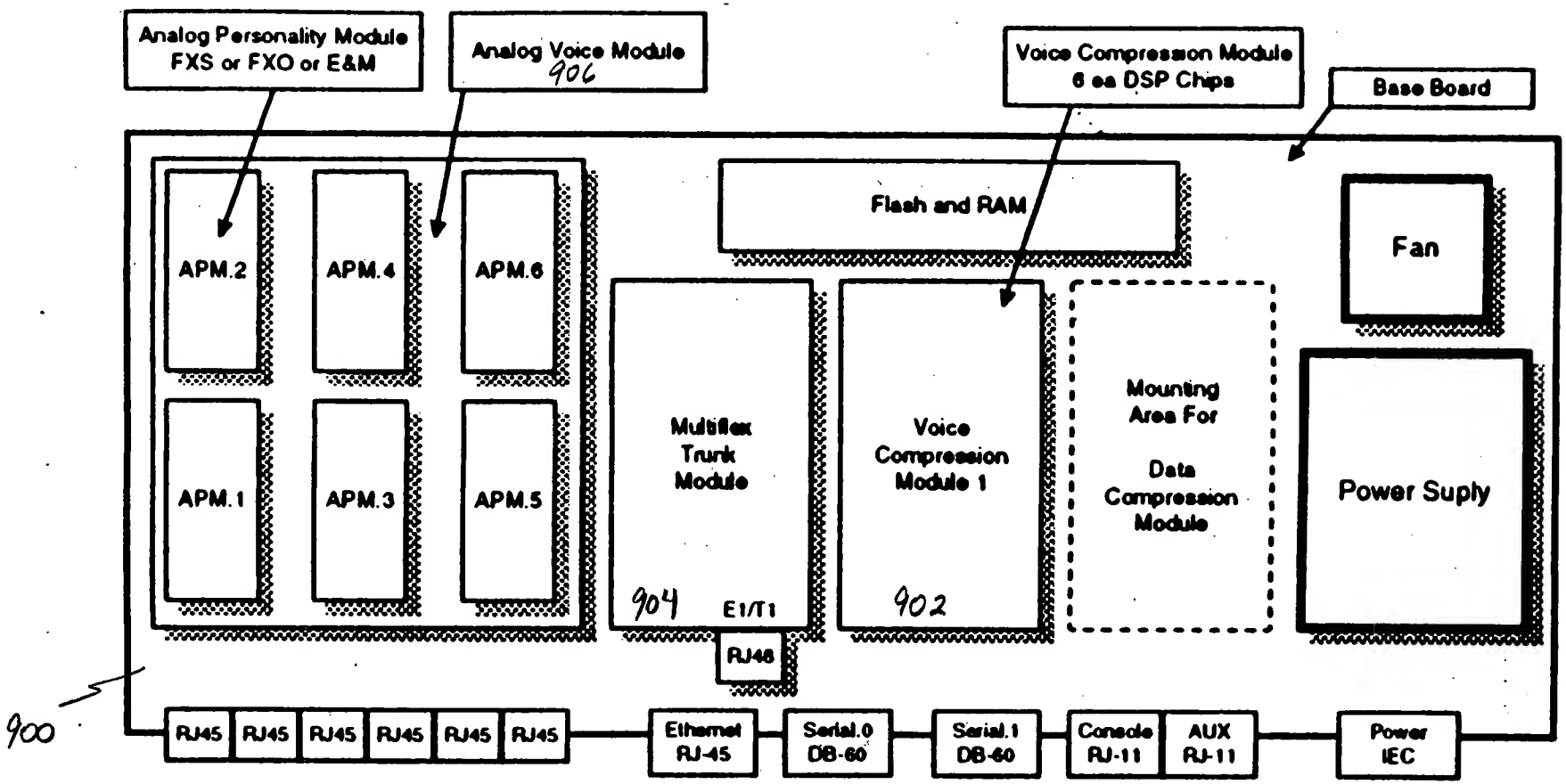


FIGURE 9

860E60" 92hh9T60

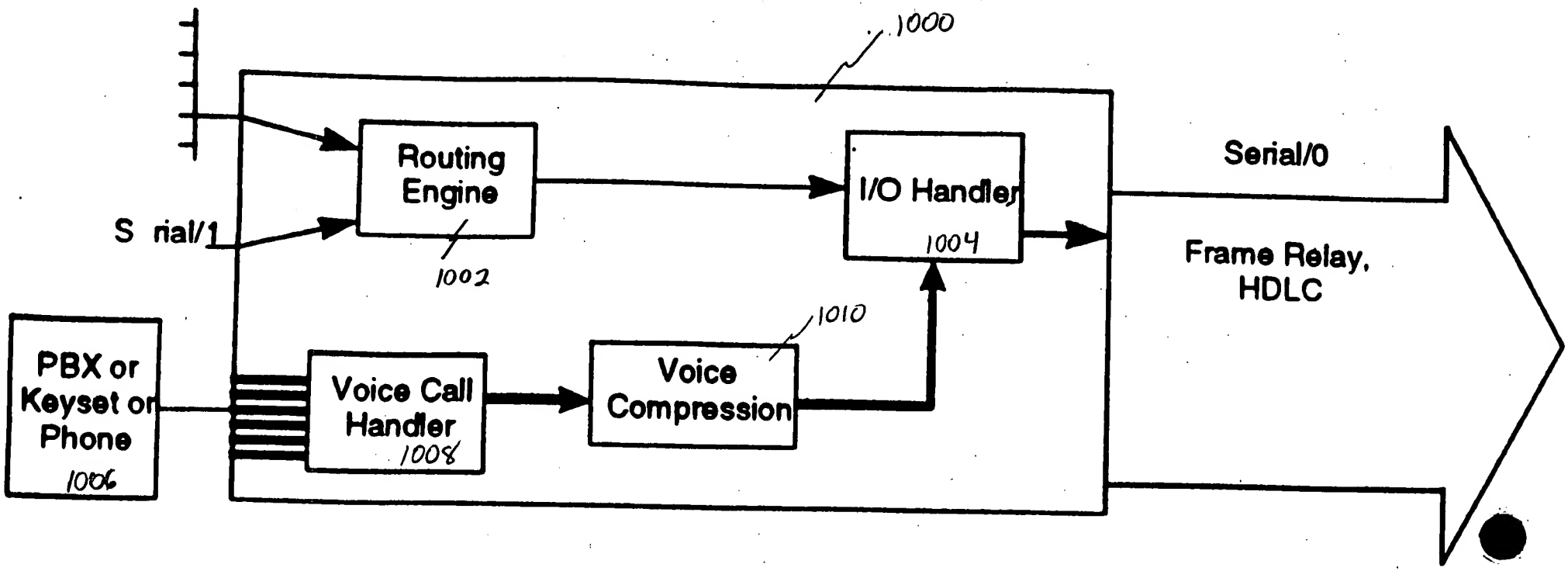


FIGURE 10

860E60 92h9T60

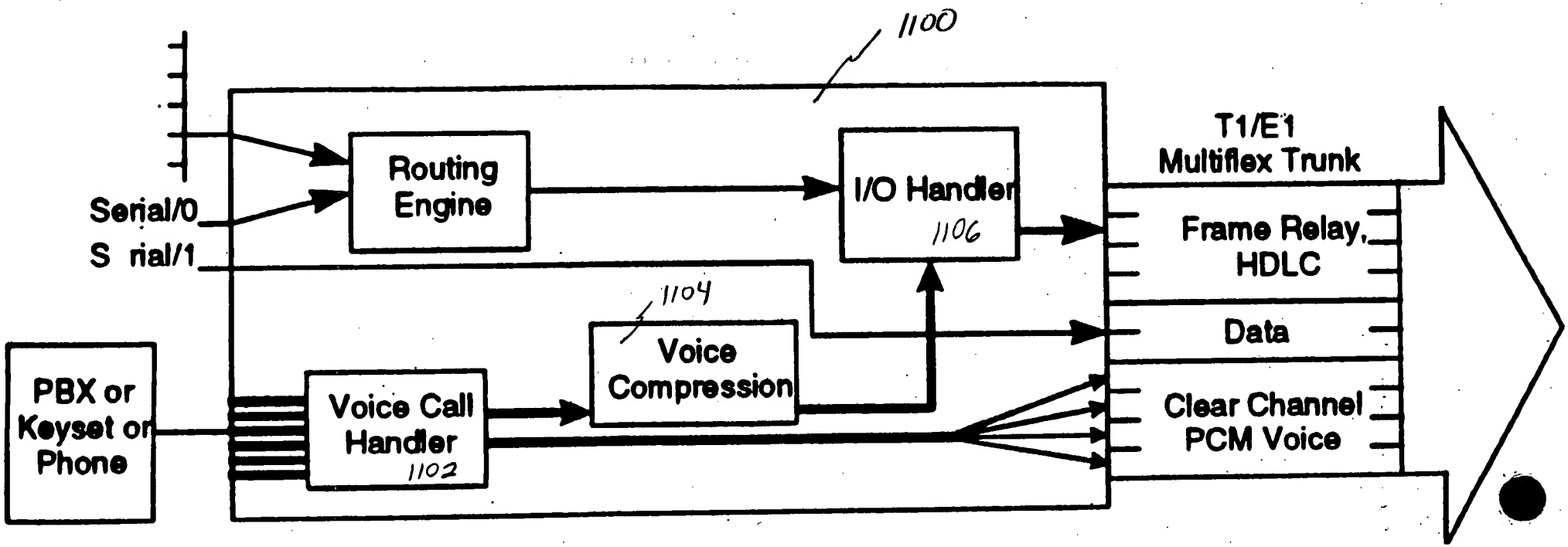


FIGURE 11

860E60" 92hh9T60

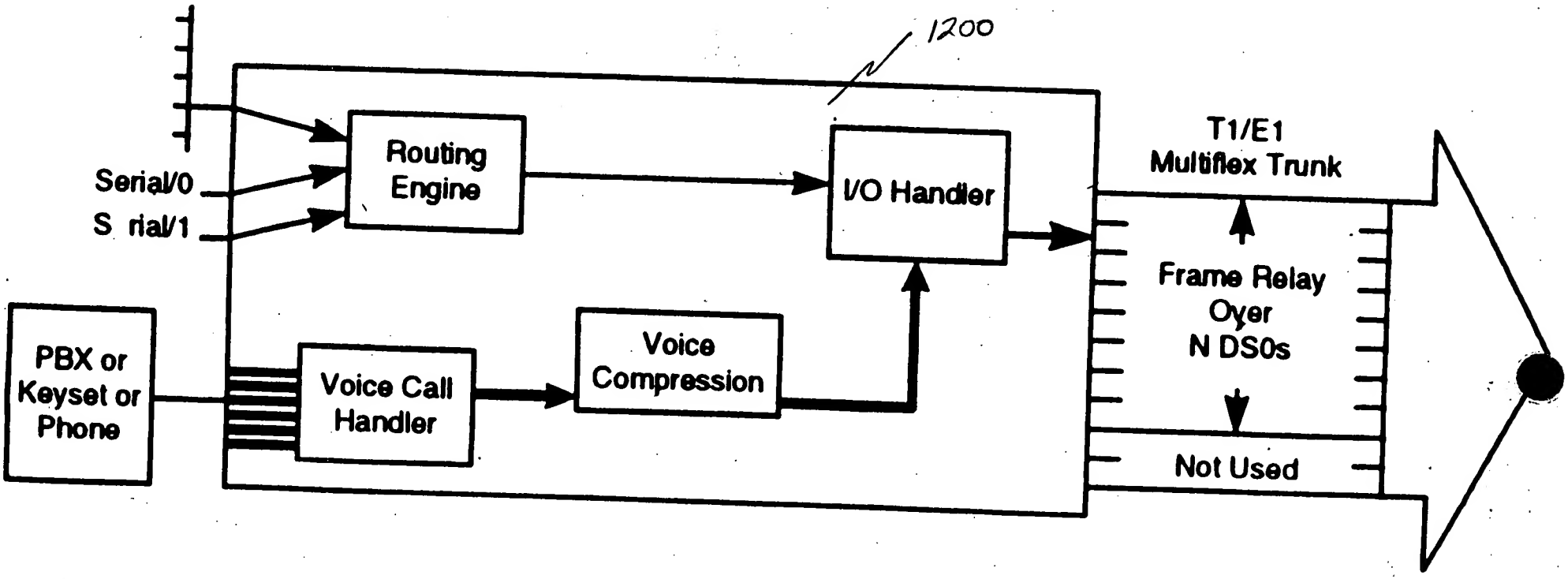


FIGURE 12

860660 "92h9T60

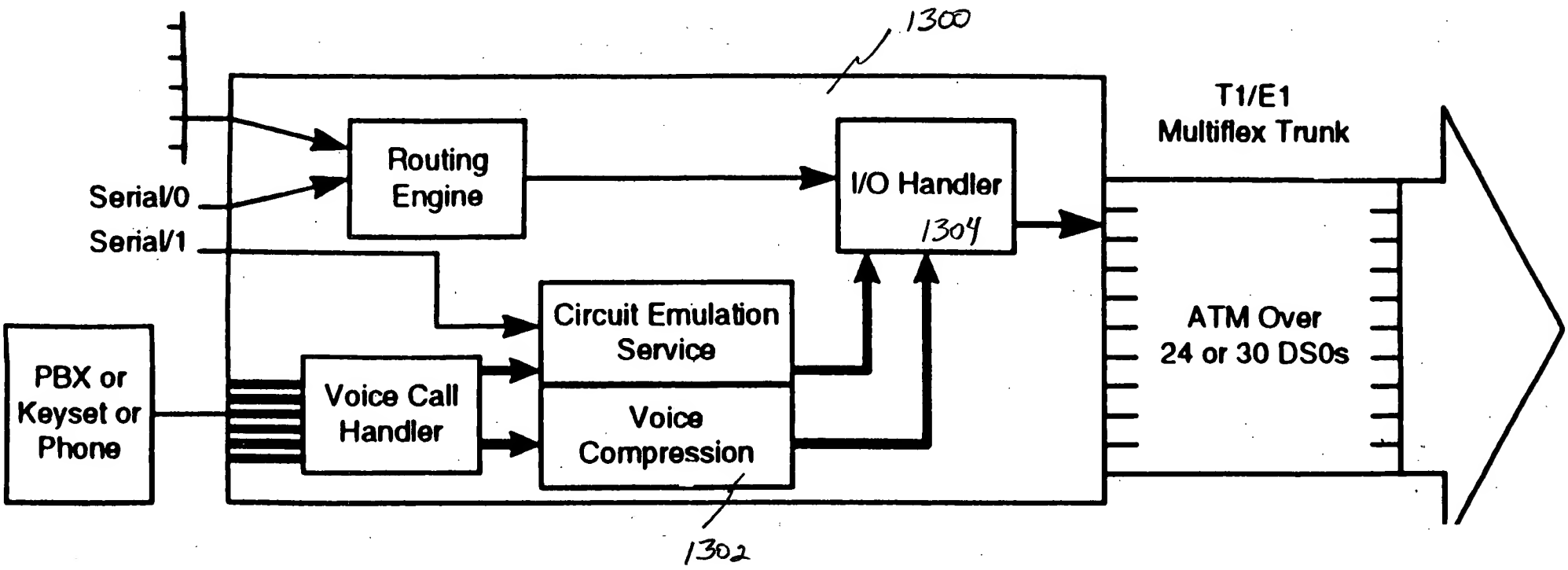


FIGURE 13

860E60" 92h9T60

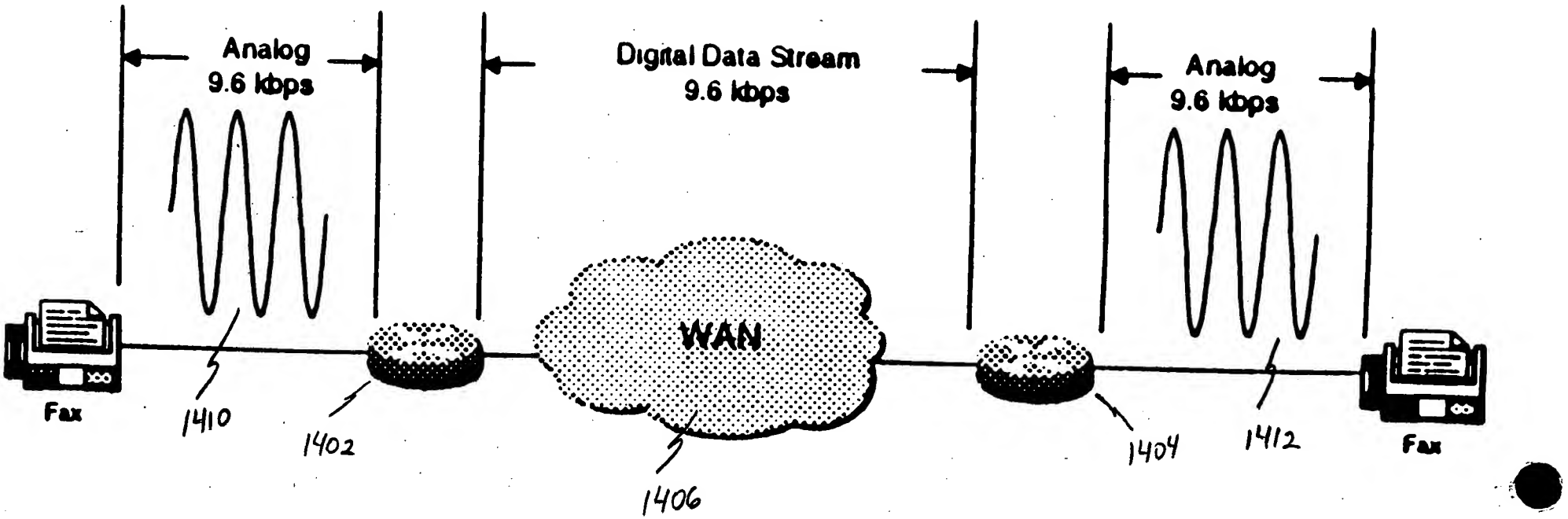


FIGURE 14

86E60" 92h9T60

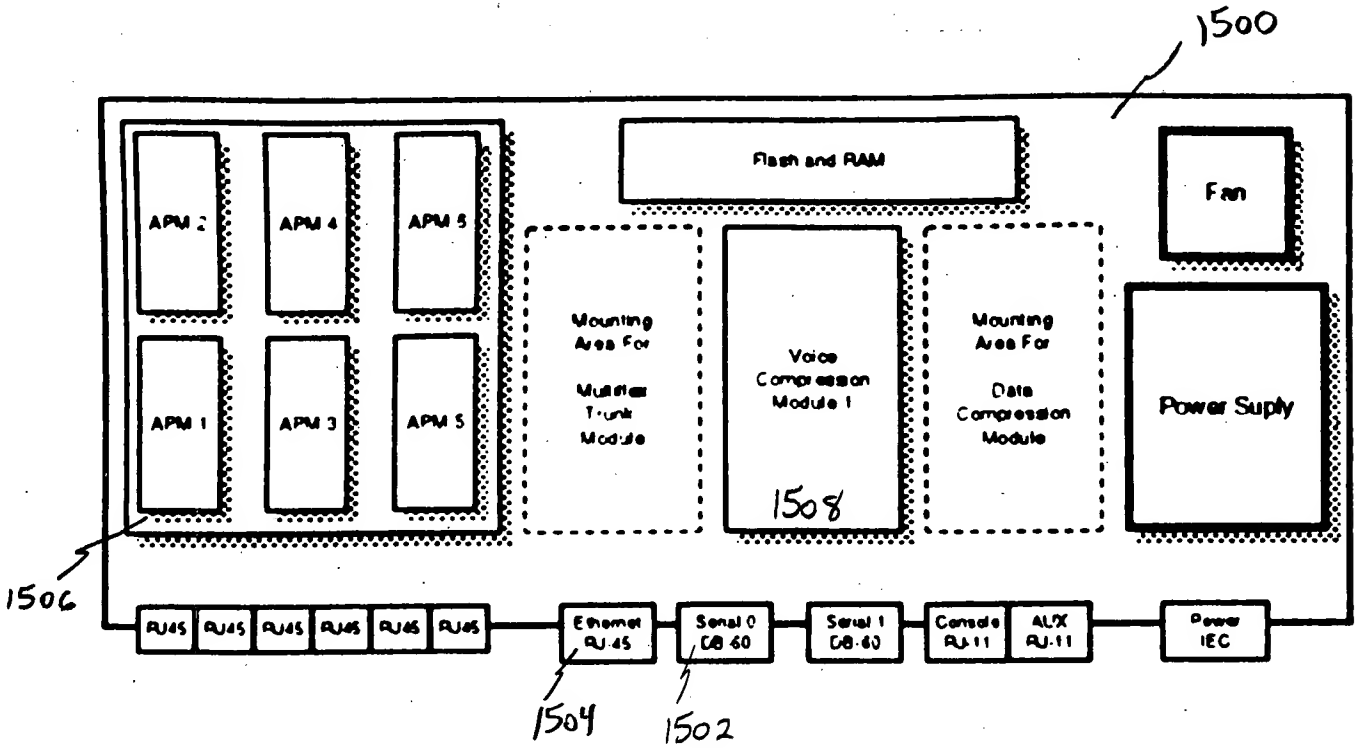


FIGURE 15

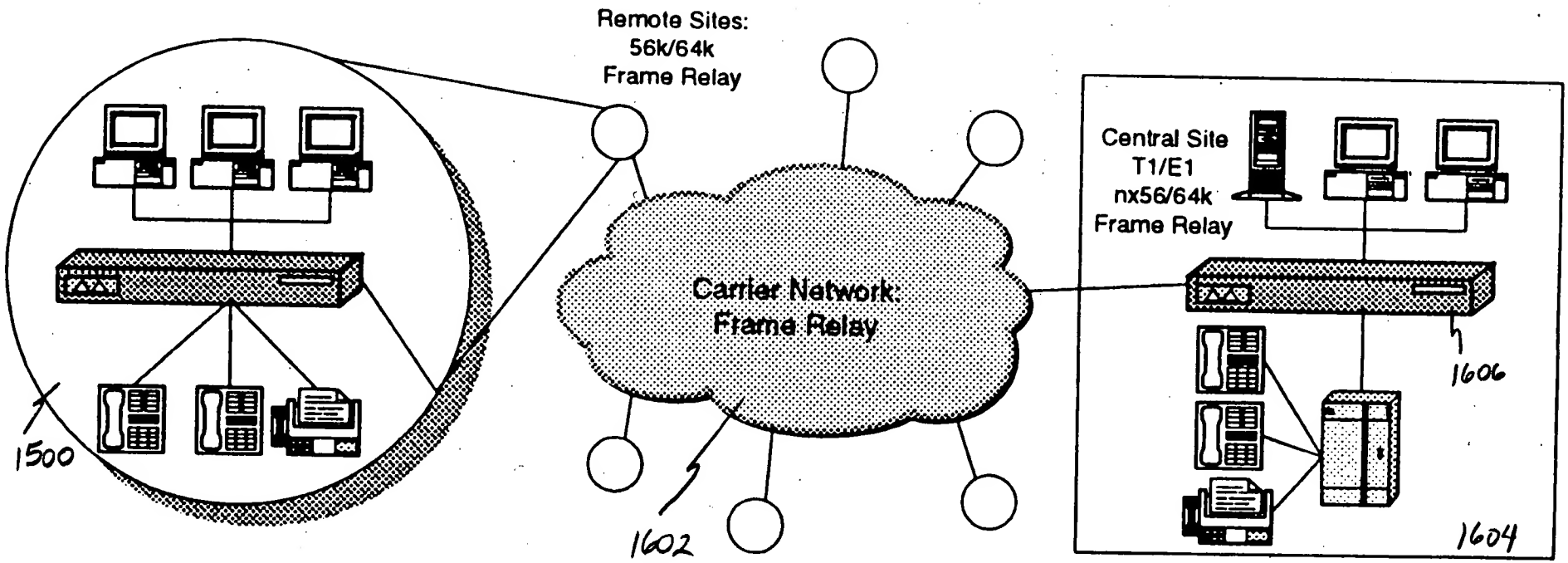

Remote Sites:
56k/64k
Frame Relay
Carrier Network:
Frame Relay
Central Site
T1/E1
nx56/64k
Frame Relay
1500
1602
1604
1606

FIGURE 16

860E60" 92hh9T60

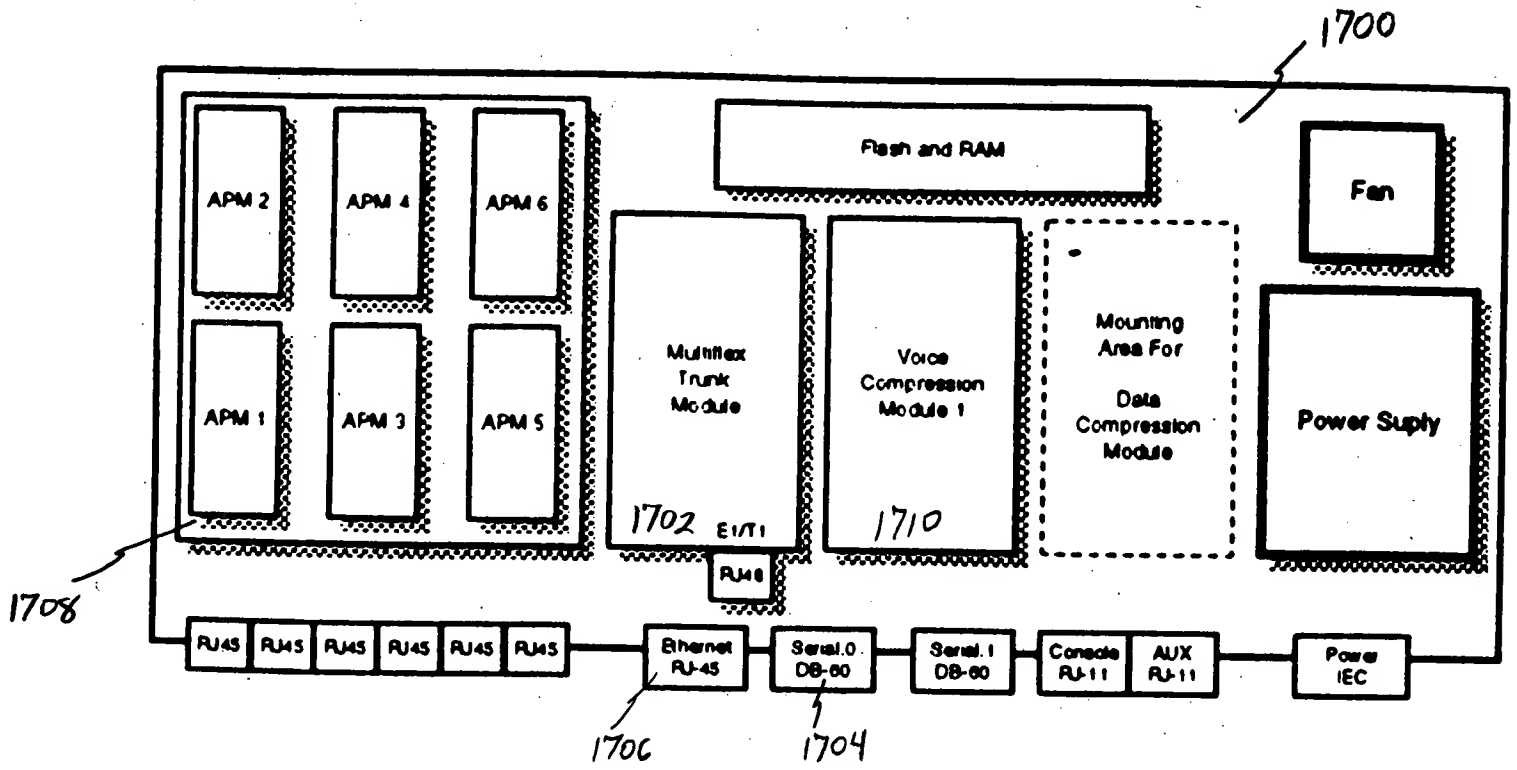


FIGURE 17

860660 "92h9160

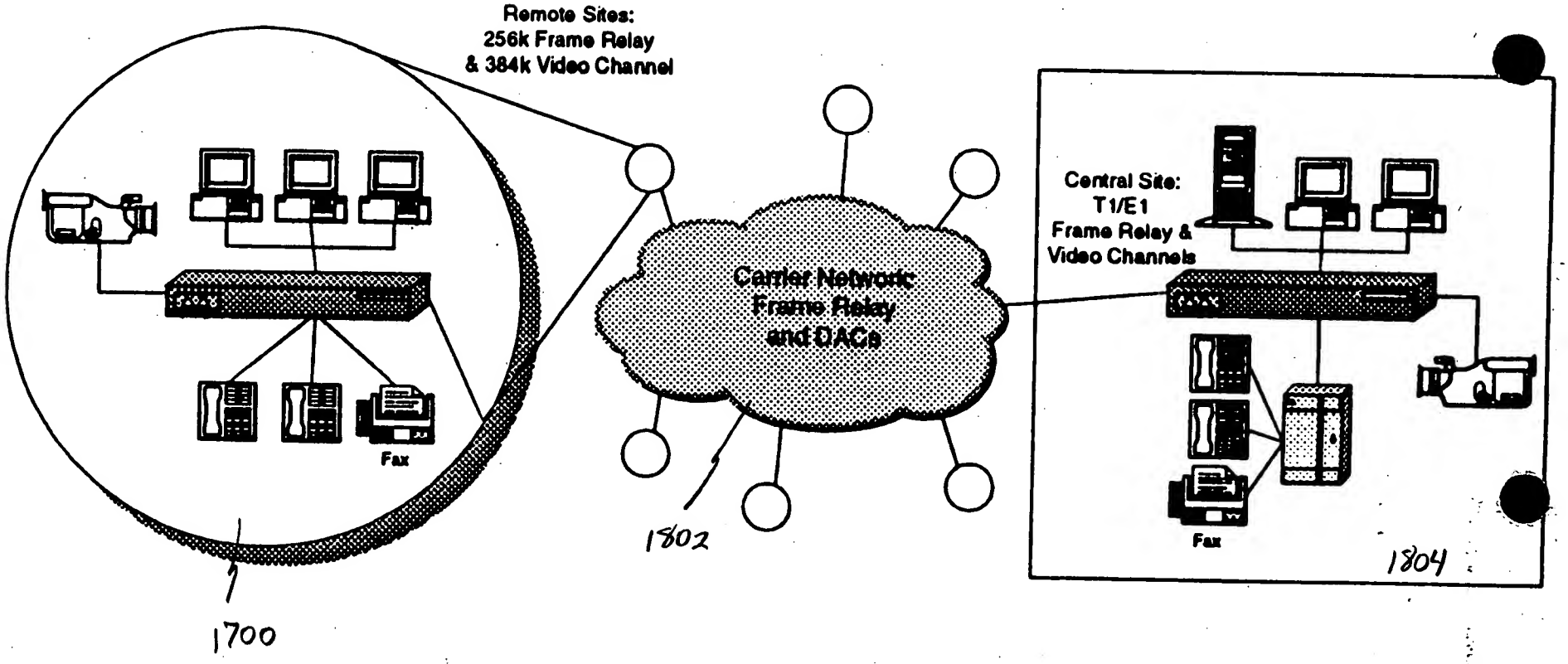


FIGURE 18

860660 "92h9T60

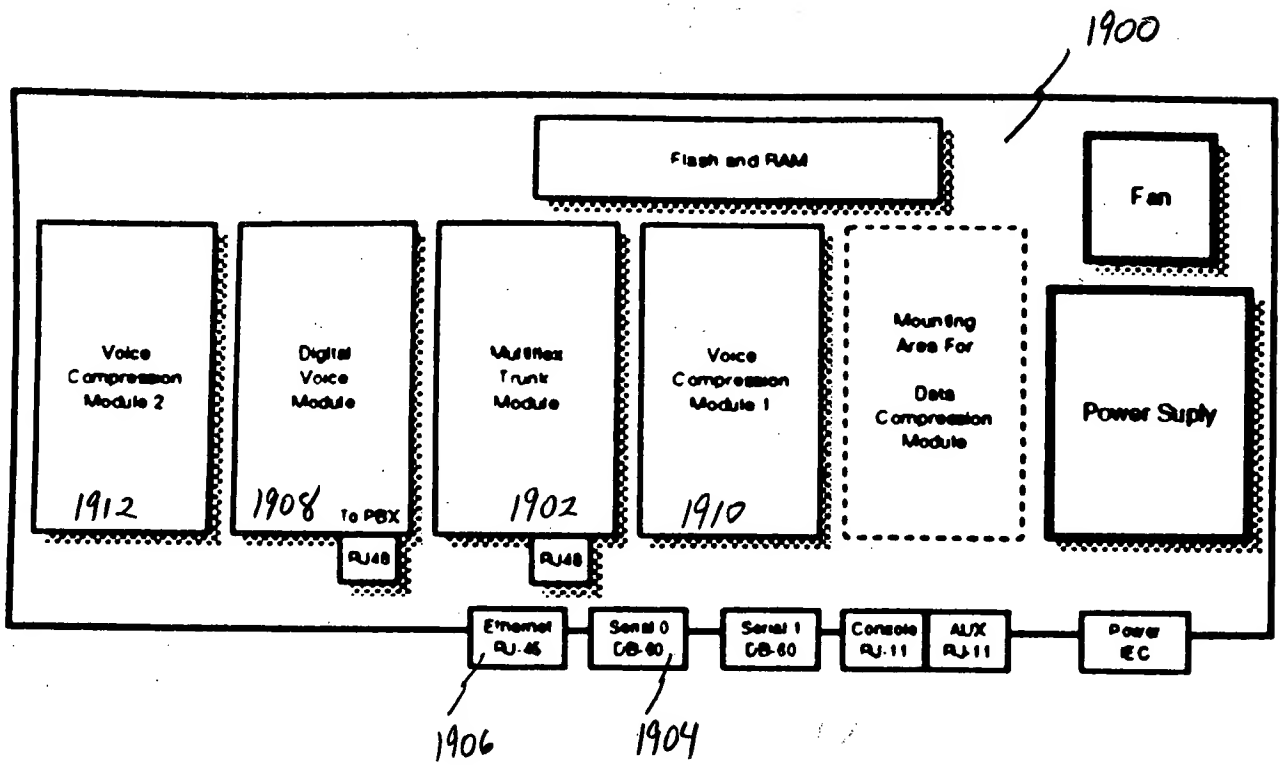


FIGURE 19

860E60" 92nh9T60

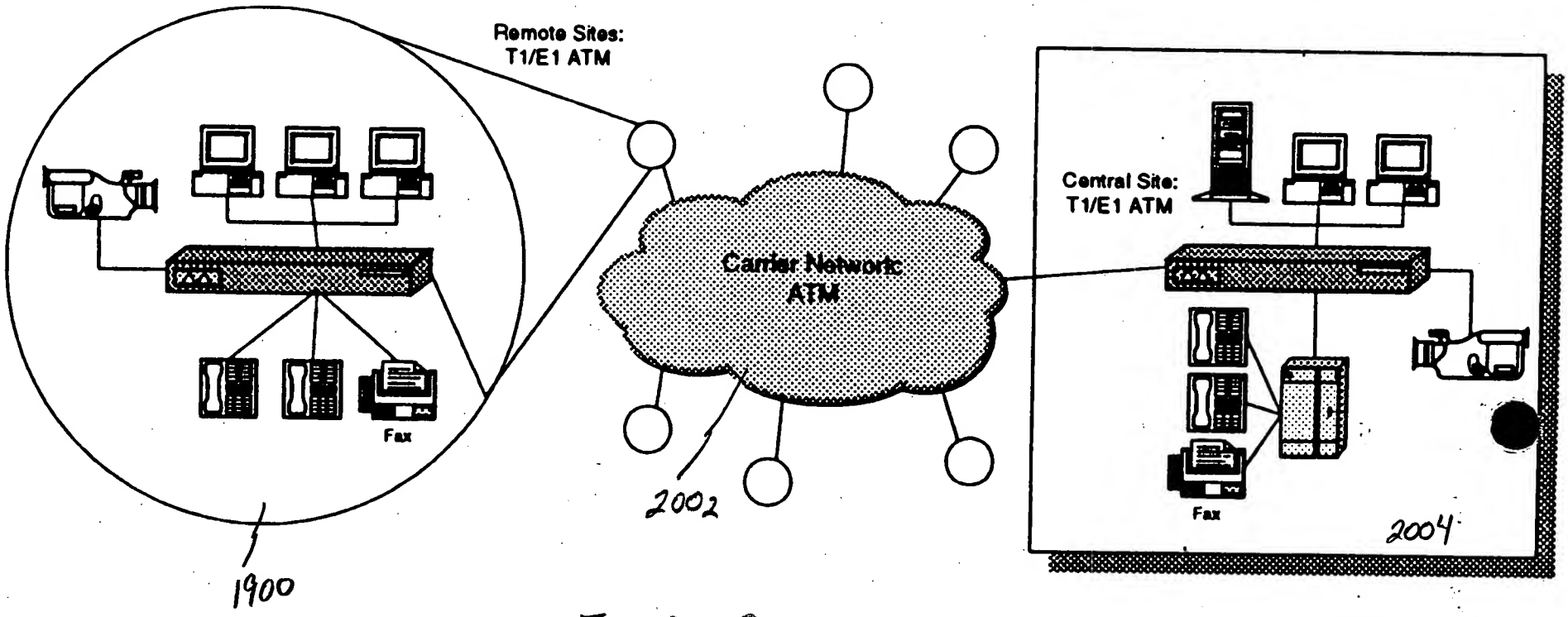


FIGURE 20

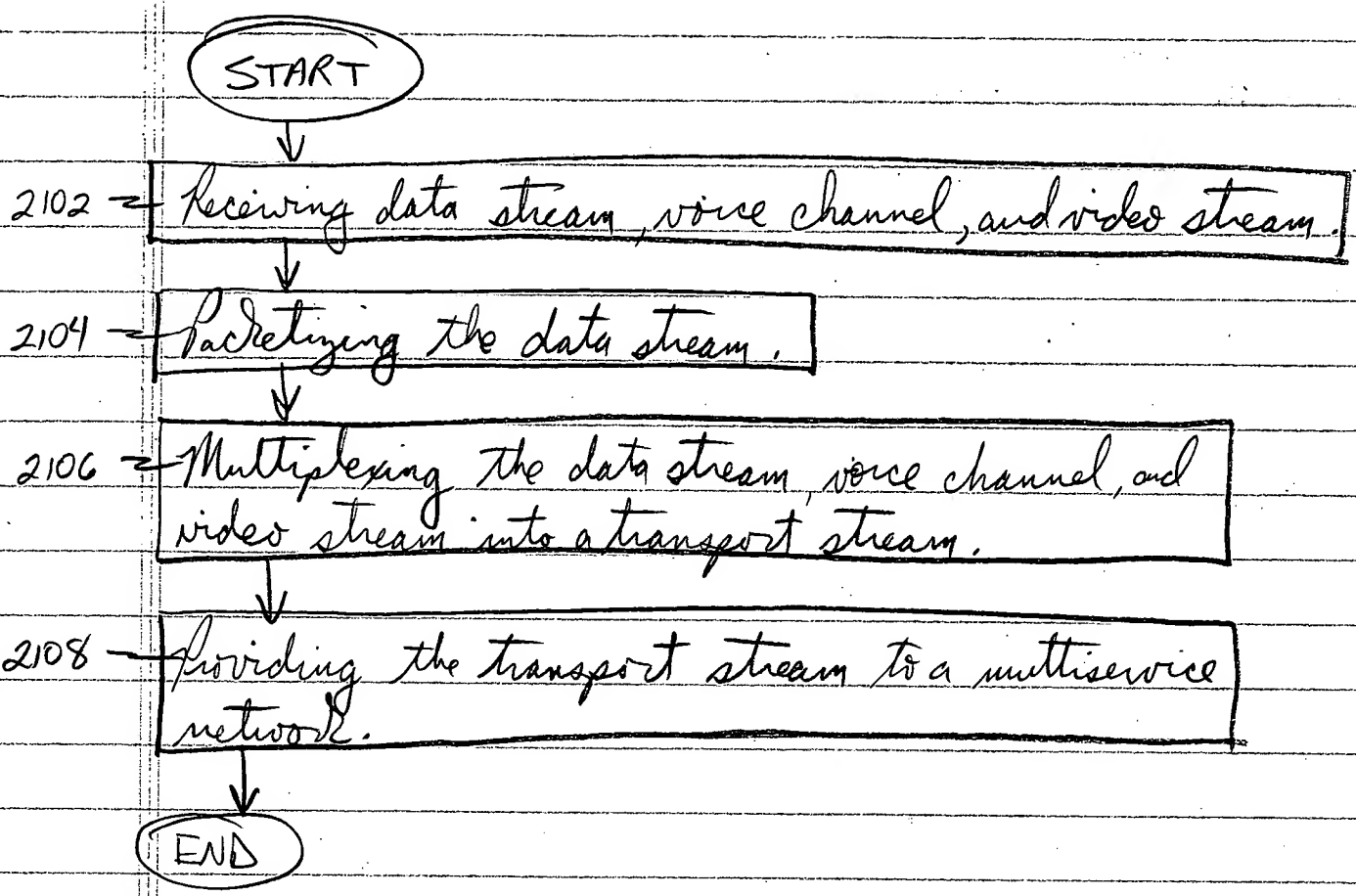

START
2102
Receiving data stream, voice channel, and video stream.
2104
Packetizing the data stream.
2106
Multiplexing the data stream, voice channel, and video stream into a transport stream.
2108
Providing the transport stream to a multiservice network.
END

FIGURE 21

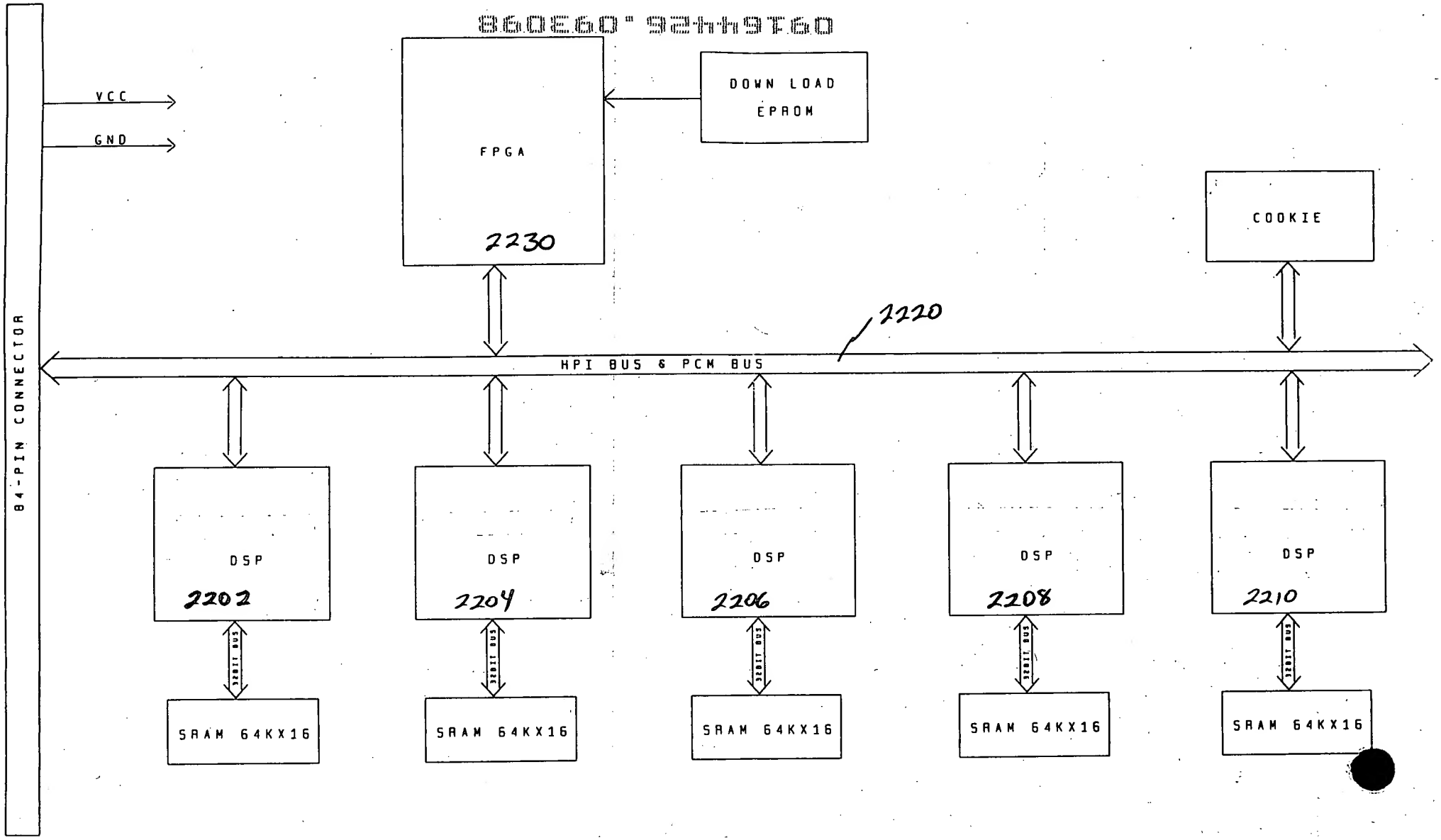

VCC
GND
FPGA
2230
DOWN LOAD
EPROM
COOKIE
2220
HPI BUS & PCM BUS
84-PIN CONNECTOR
DSP
2202
DSP
2204
DSP
2206
DSP
2208
DSP
2210
32BIT BUS
SRAM 64KX16
SRAM 64KX16
SRAM 64KX16
SRAM 64KX16
SRAM 64KX16

FIGURE 22

860E60 92th9T60

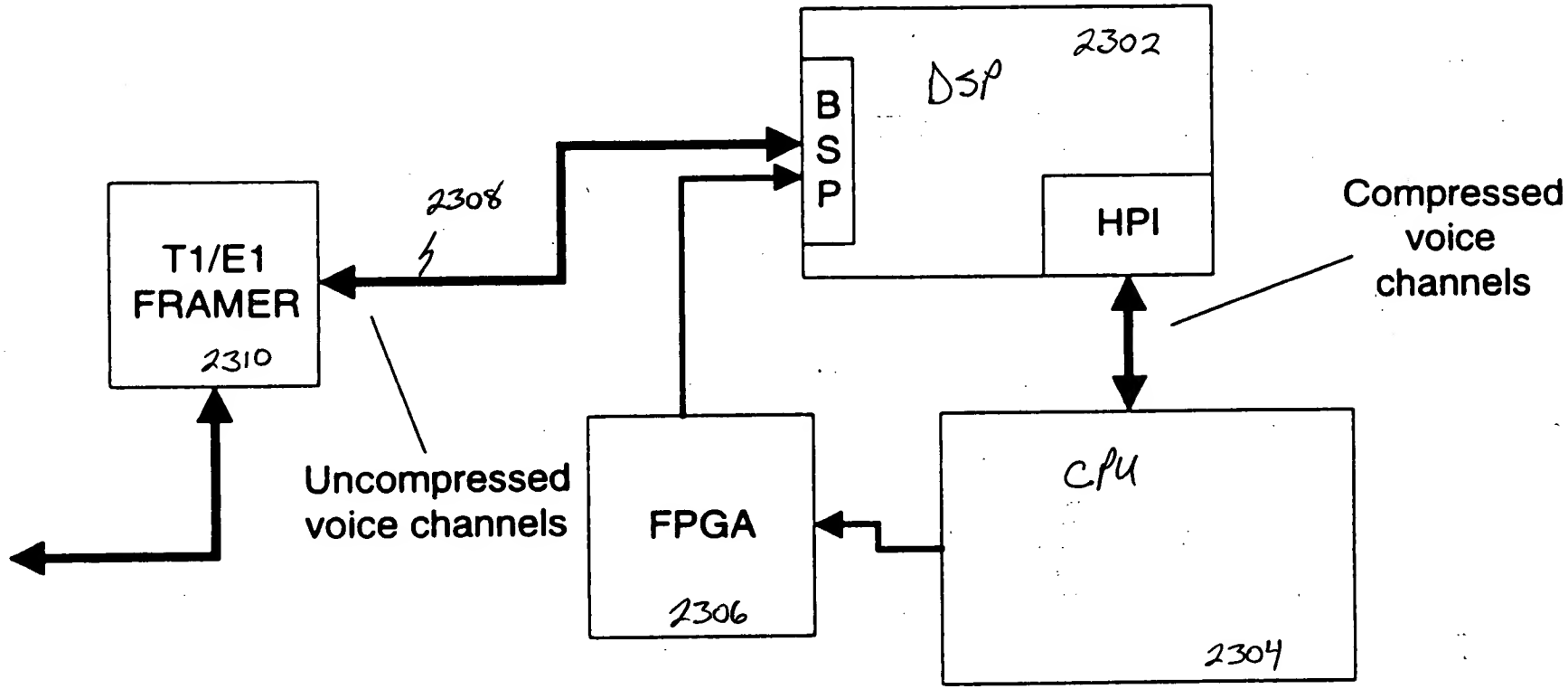


FIGURE 23

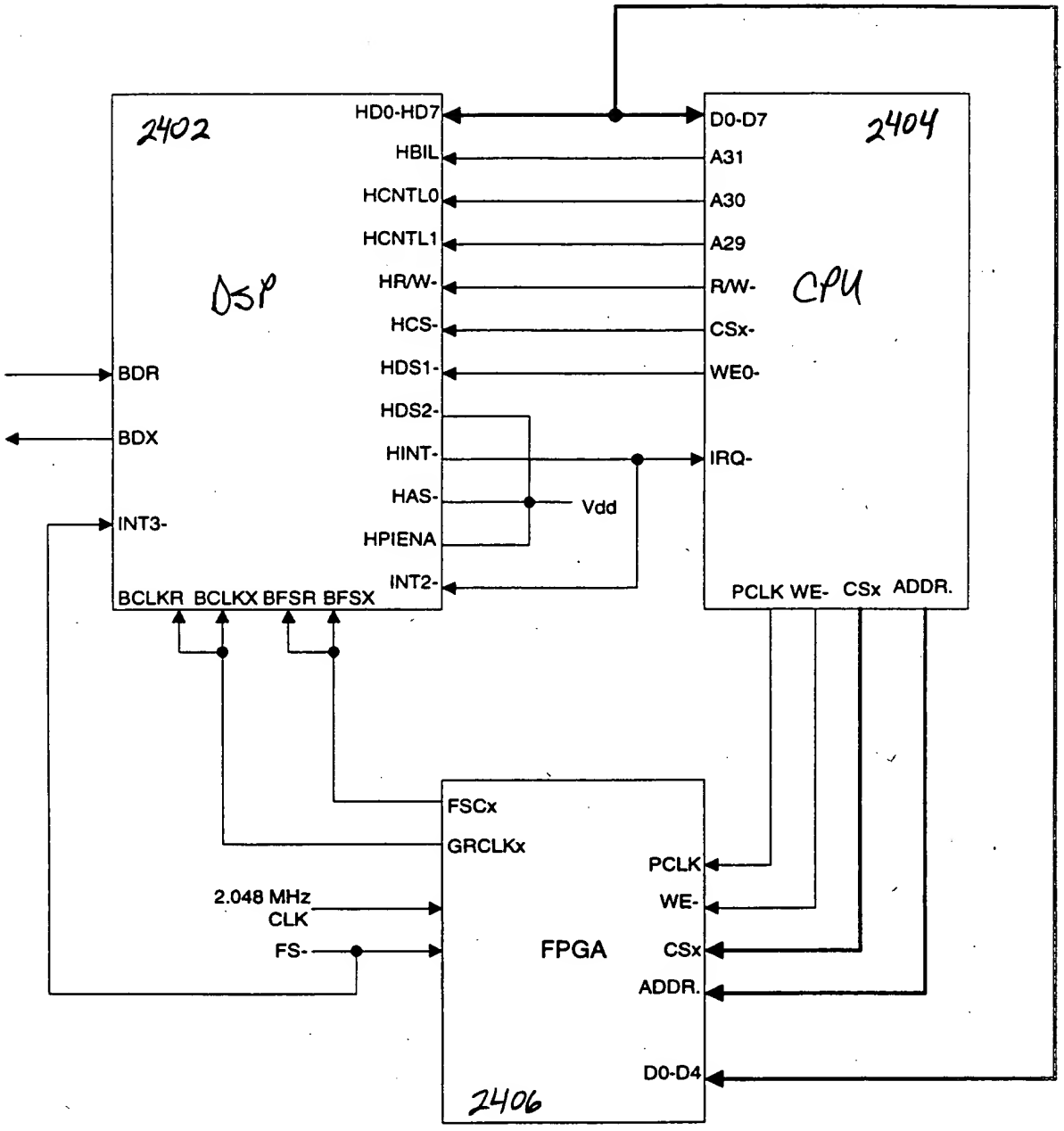

2402
DSP
HD0-HD7
HBIL
HCNTL0
HCNTL1
HR/W-
HCS-
HDS1-
HDS2-
HINT-
HAS-
HPIENA
INT2-
BDR
BDX
INT3-
BCLKR BCLKX BFSR BFSX
Vdd
2404
CPU
D0-D7
A31
A30
A29
R/W-
CSx-
WE0-
IRQ-
PCLK WE- CSx ADDR.
FSCx
GRCLKx
2.048 MHz CLK
FS-
FPGA
PCLK
WE-
CSx
ADDR.
D0-D4
2406

FIGURE 24

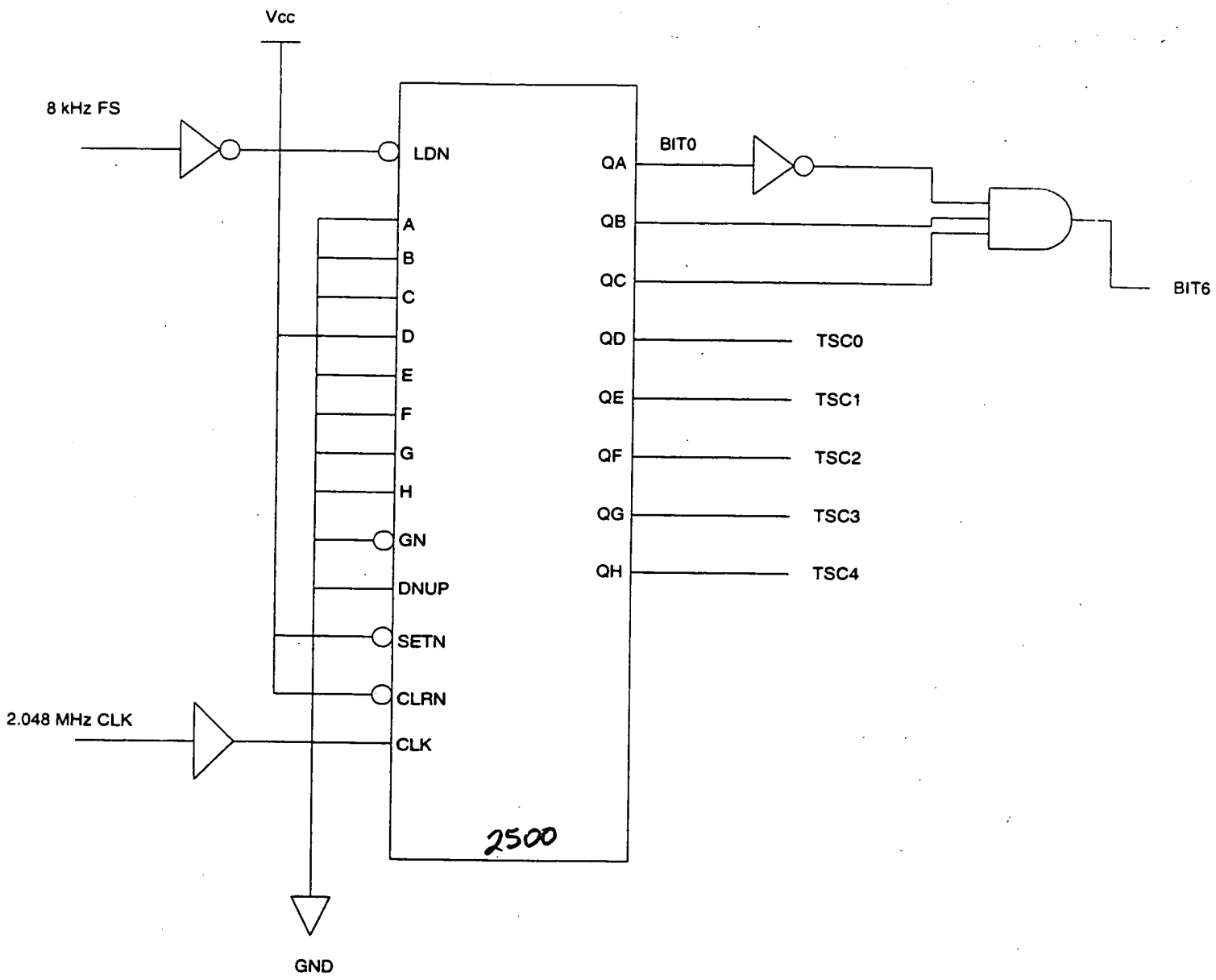

Vcc
8 kHz FS
LDN
A
B
C
D
E
F
G
H
GN
DNUP
SETN
CLRN
2.048 MHz CLK
CLK
2500
GND
QA
QB
QC
QD
QE
QF
QG
QH
BIT0
BIT6
TSC0
TSC1
TSC2
TSC3
TSC4

FIGURE 25

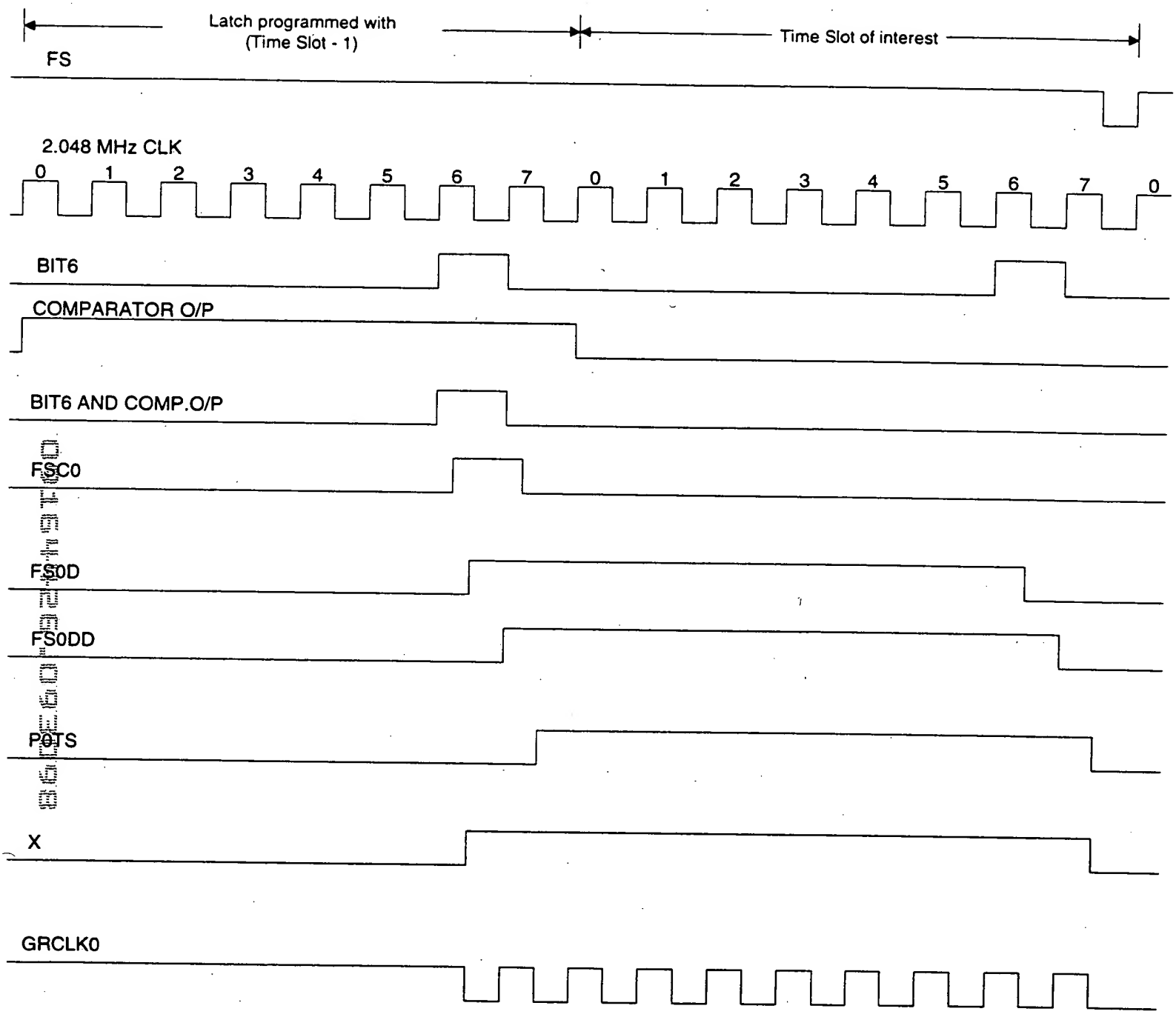

Latch programmed with
(Time Slot - 1)
Time Slot of interest
FS
2.048 MHz CLK
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0
BIT6
COMPARATOR O/P
BIT6 AND COMP.O/P
FSC0
FS0D
FS0DD
P0TS
X
GRCLK0

FIGURE 26

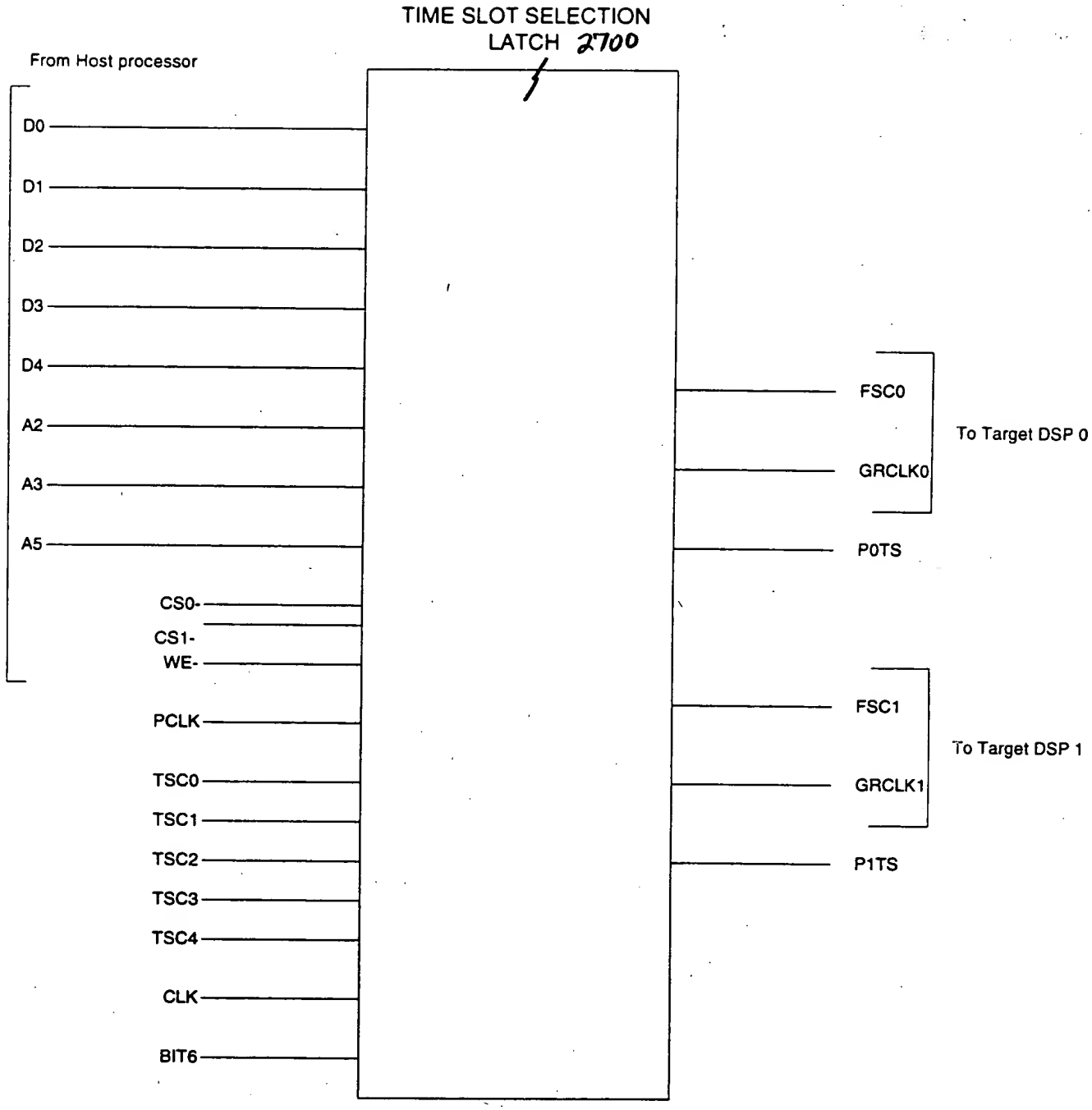

TIME SLOT SELECTION
LATCH 2700
From Host processor
D0
D1
D2
D3
D4
A2
A3
A5
CS0-
CS1-
WE-
PCLK
TSC0
TSC1
TSC2
TSC3
TSC4
CLK
BIT6
FSC0
GRCLK0
P0TS
To Target DSP 0
FSC1
GRCLK1
P1TS
To Target DSP 1

FIGURE 27

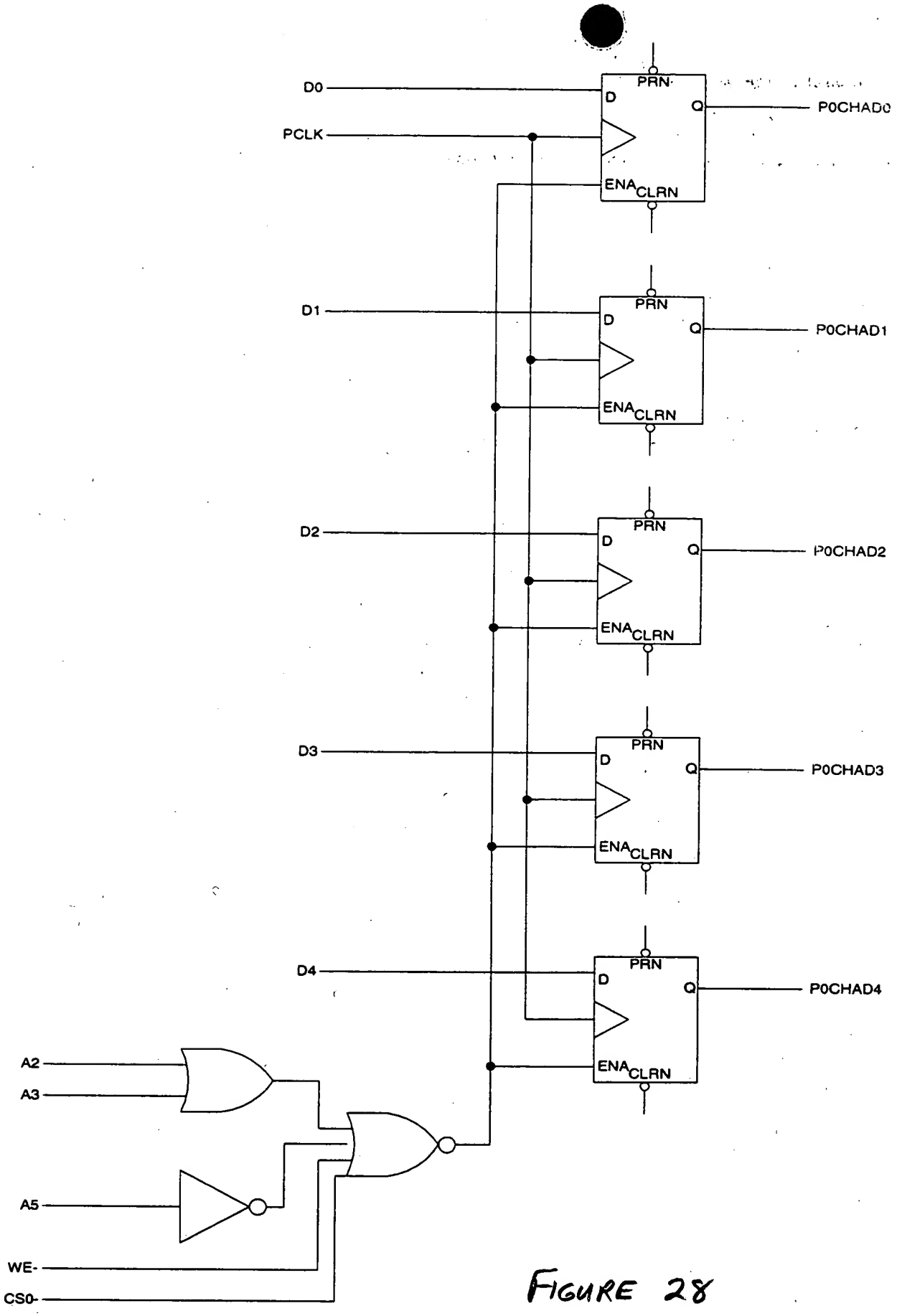

D0
PCLK
PRN
D
Q
ENA
CLRN
P0CHAD0
D1
P0CHAD1
D2
P0CHAD2
D3
P0CHAD3
D4
P0CHAD4
A2
A3
A5
WE-
CS0-

FIGURE 28

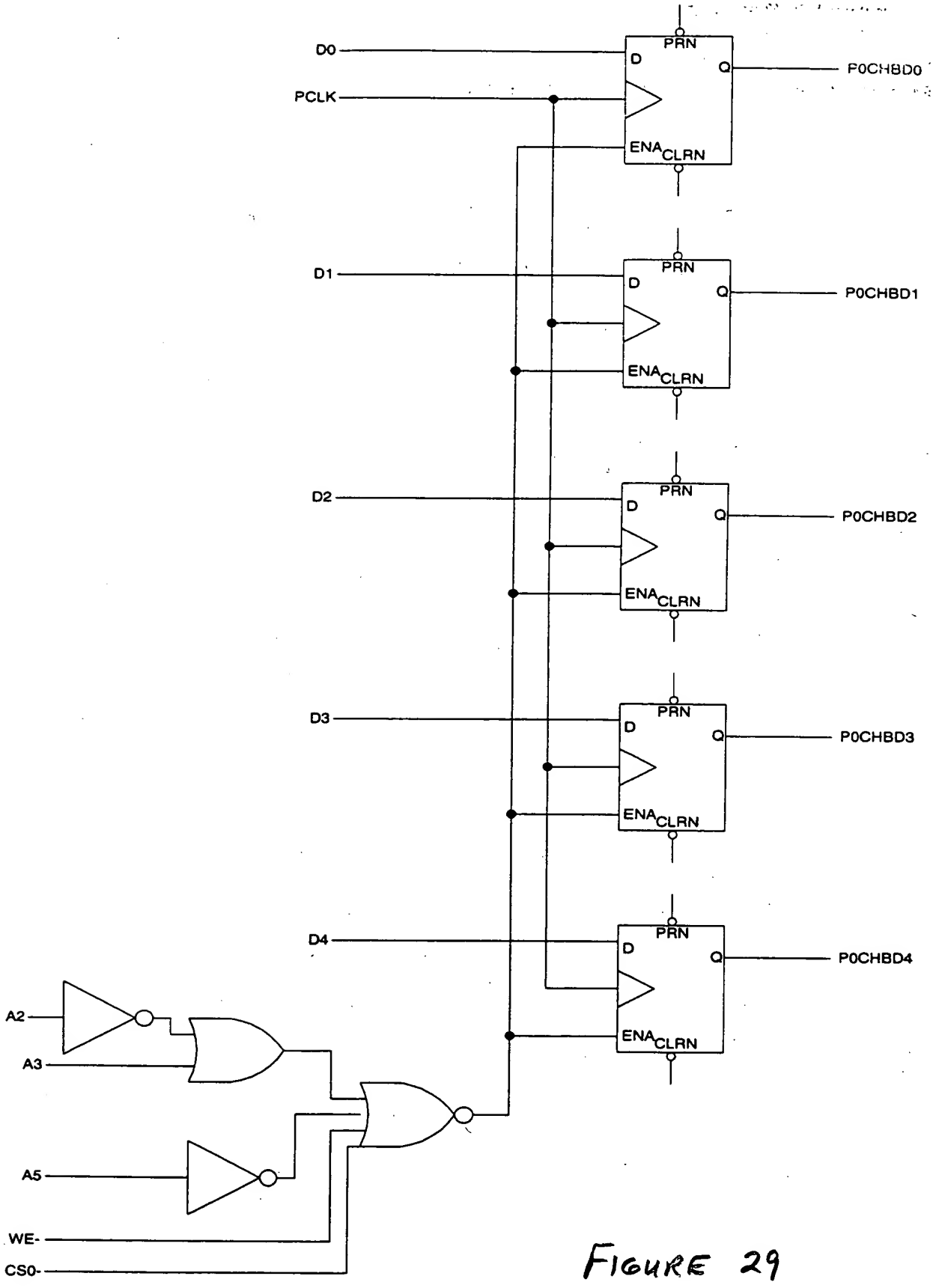

D0
PCLK
PRN
D
Q
ENA
CLRN
P0CHBD0
D1
P0CHBD1
D2
P0CHBD2
D3
P0CHBD3
D4
P0CHBD4
A2
A3
A5
WE-
CS0-

FIGURE 29

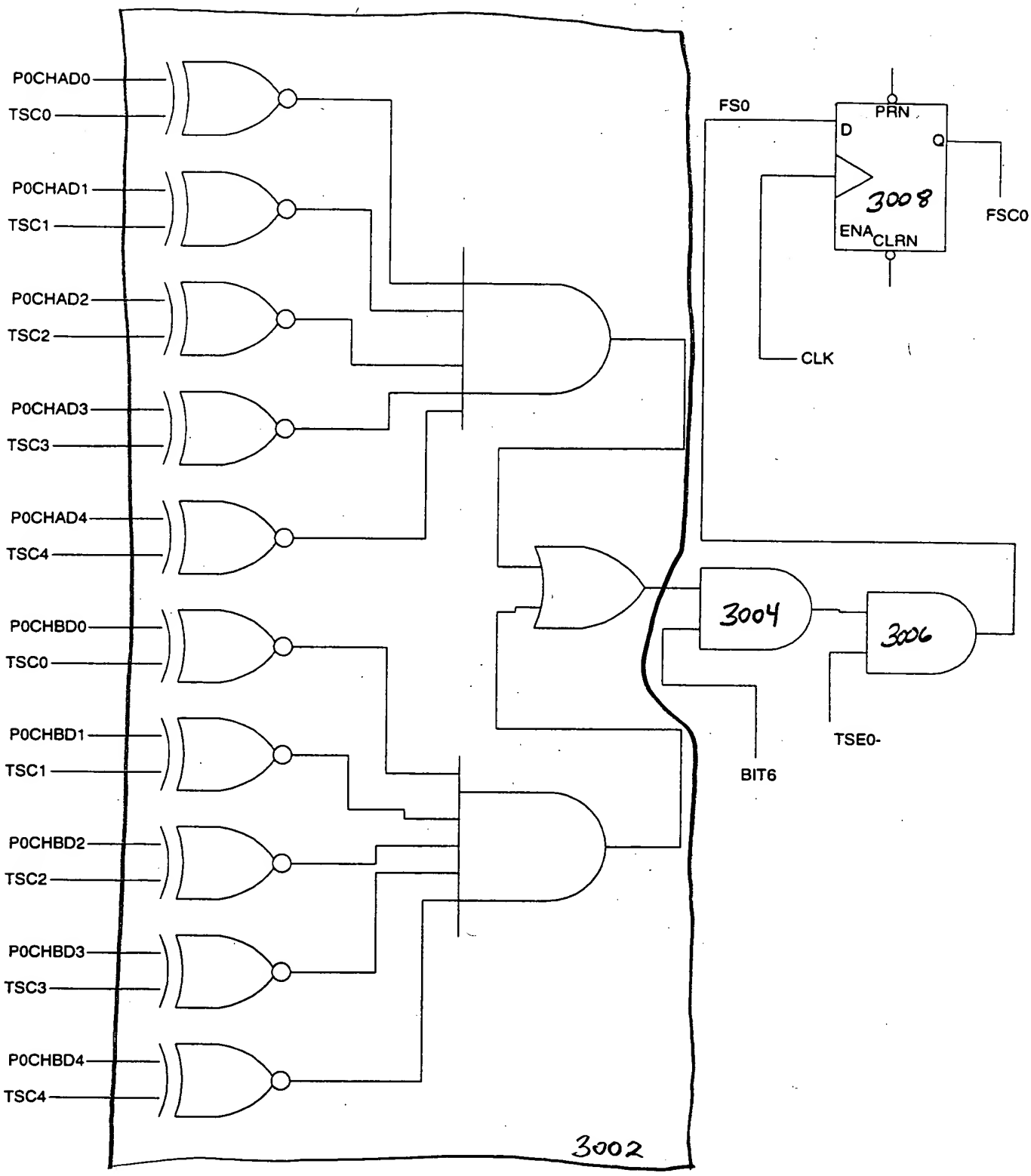
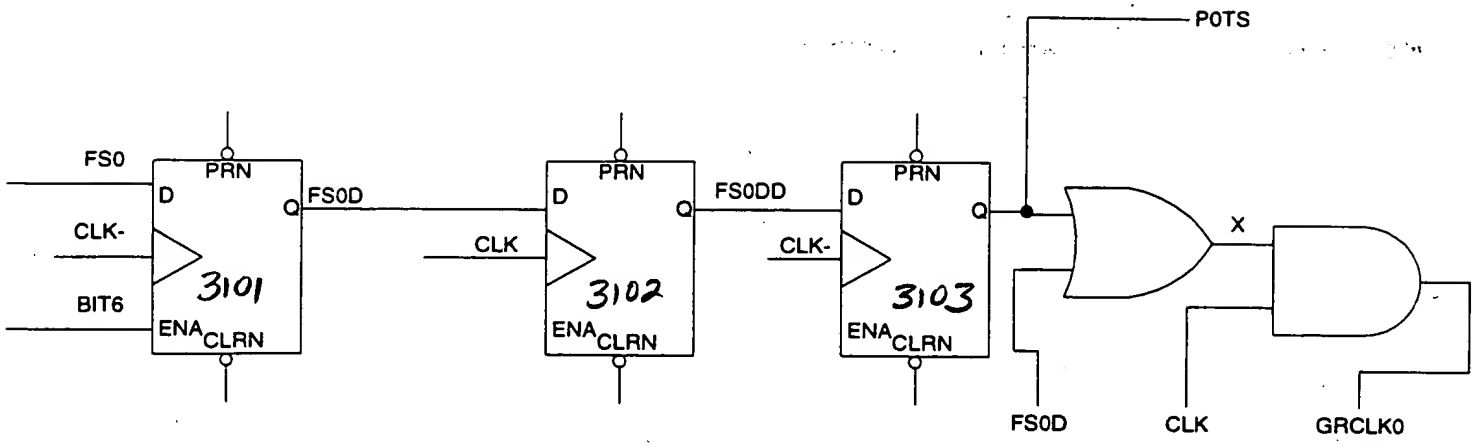
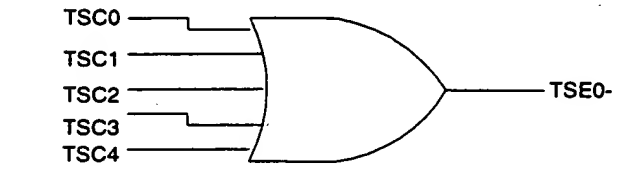

P0CHAD0
TSC0
P0CHAD1
TSC1
P0CHAD2
TSC2
P0CHAD3
TSC3
P0CHAD4
TSC4
P0CHBD0
TSC0
P0CHBD1
TSC1
P0CHBD2
TSC2
P0CHBD3
TSC3
P0CHBD4
TSC4
3002
FS0
PRN
D
Q
3008
ENA
CLRN
FSC0
CLK
3004
3006
TSE0-
BIT6

FIGURE 30


POTS
FS0
PRN
D
Q
FS0D
CLK-
3101
BIT6
ENA
CLRN
CLK
3102
FS0DD
CLK-
3103
X
FS0D
CLK
GRCLK0


TSC0
TSC1
TSC2
TSC3
TSC4
TSE0-

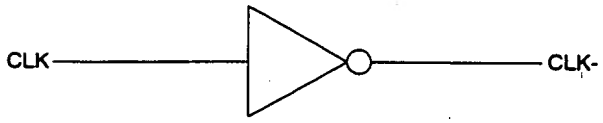

CLK
CLK-

FIGURE 31

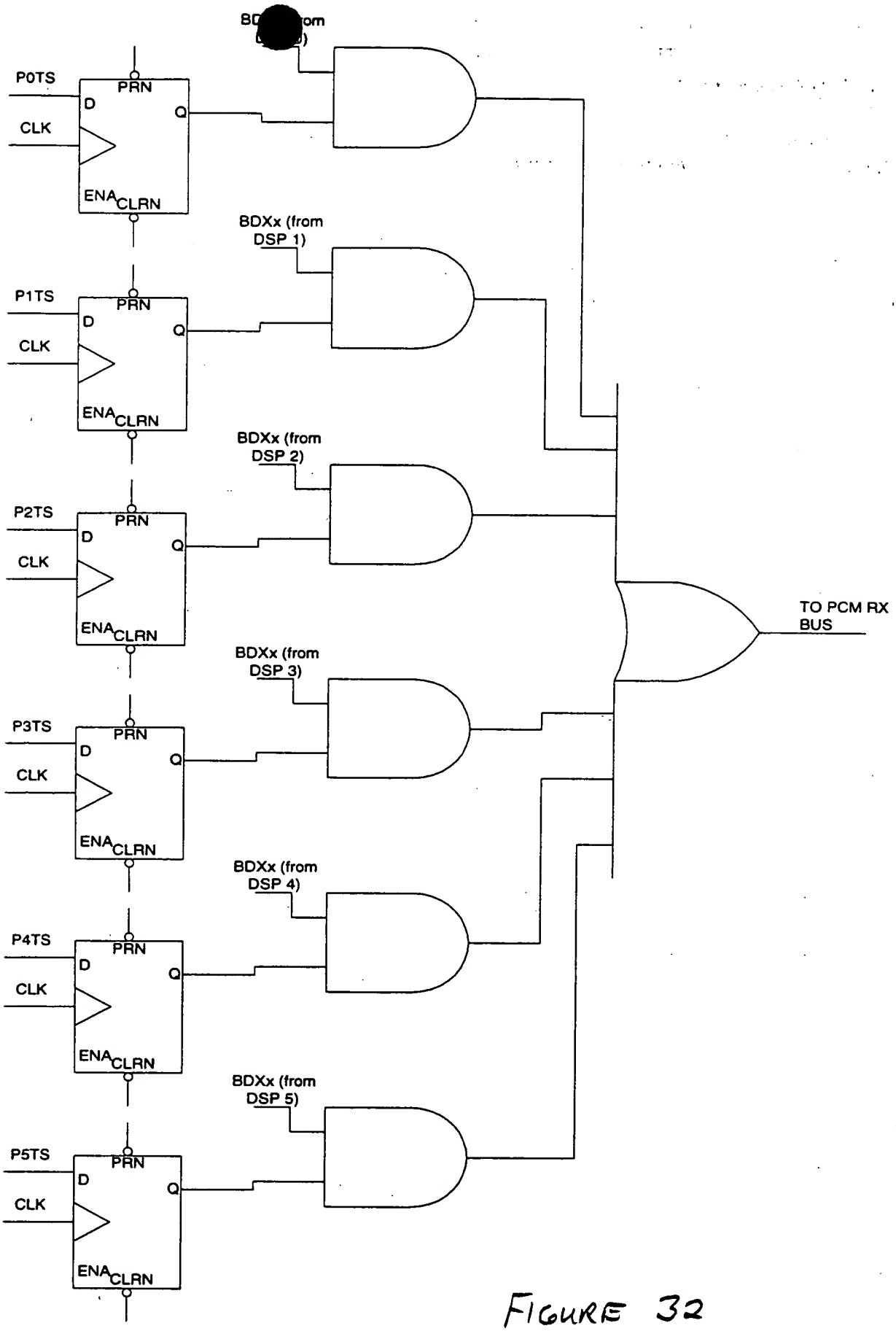

P0TS
PRN
D
Q
CLK
ENA
CLRN
BDXx (from DSP 1)
P1TS
BDXx (from DSP 2)
P2TS
BDXx (from DSP 3)
P3TS
BDXx (from DSP 4)
P4TS
BDXx (from DSP 5)
P5TS
TO PCM RX BUS

FIGURE 32

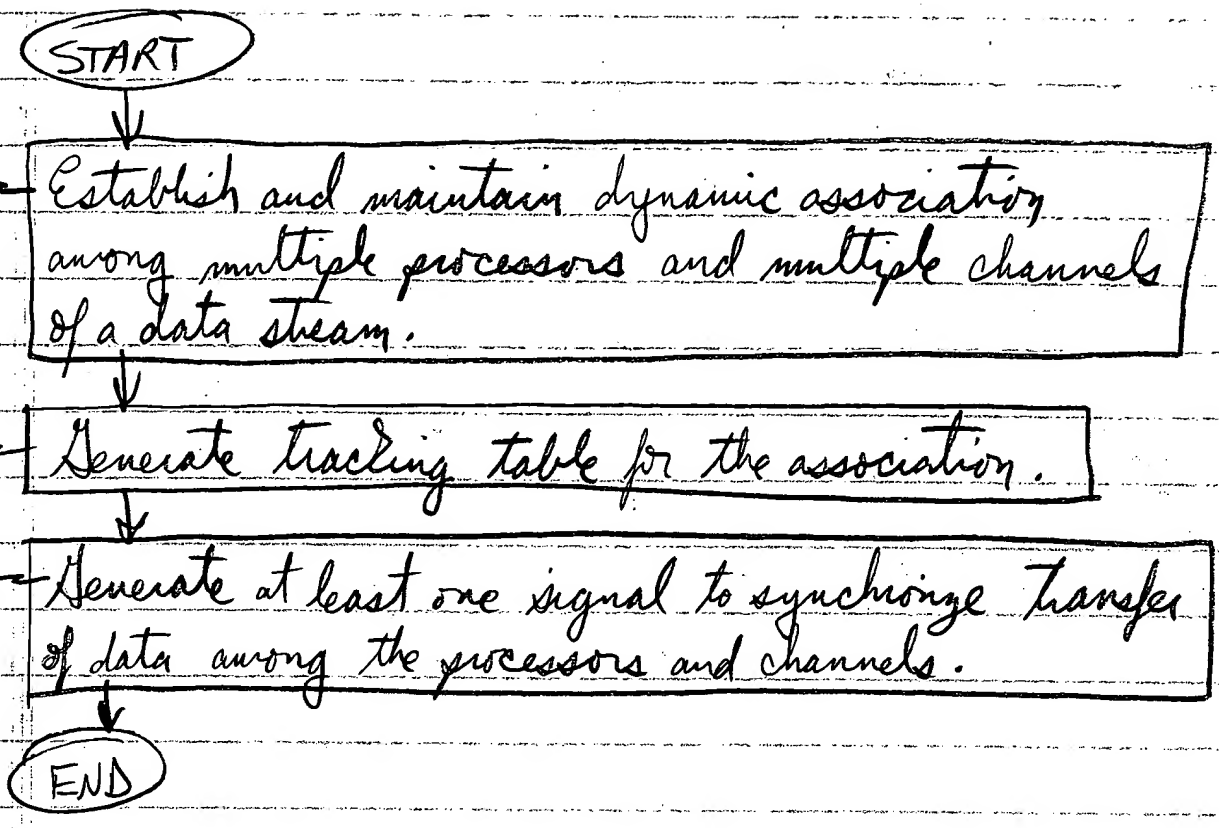

START
3302
Establish and maintain dynamic association among multiple processors and multiple channels of a data stream.
3304
Generate tracking table for the association.
3306
Generate at least one signal to synchronize transfer of data among the processors and channels.
END

FIGURE 33

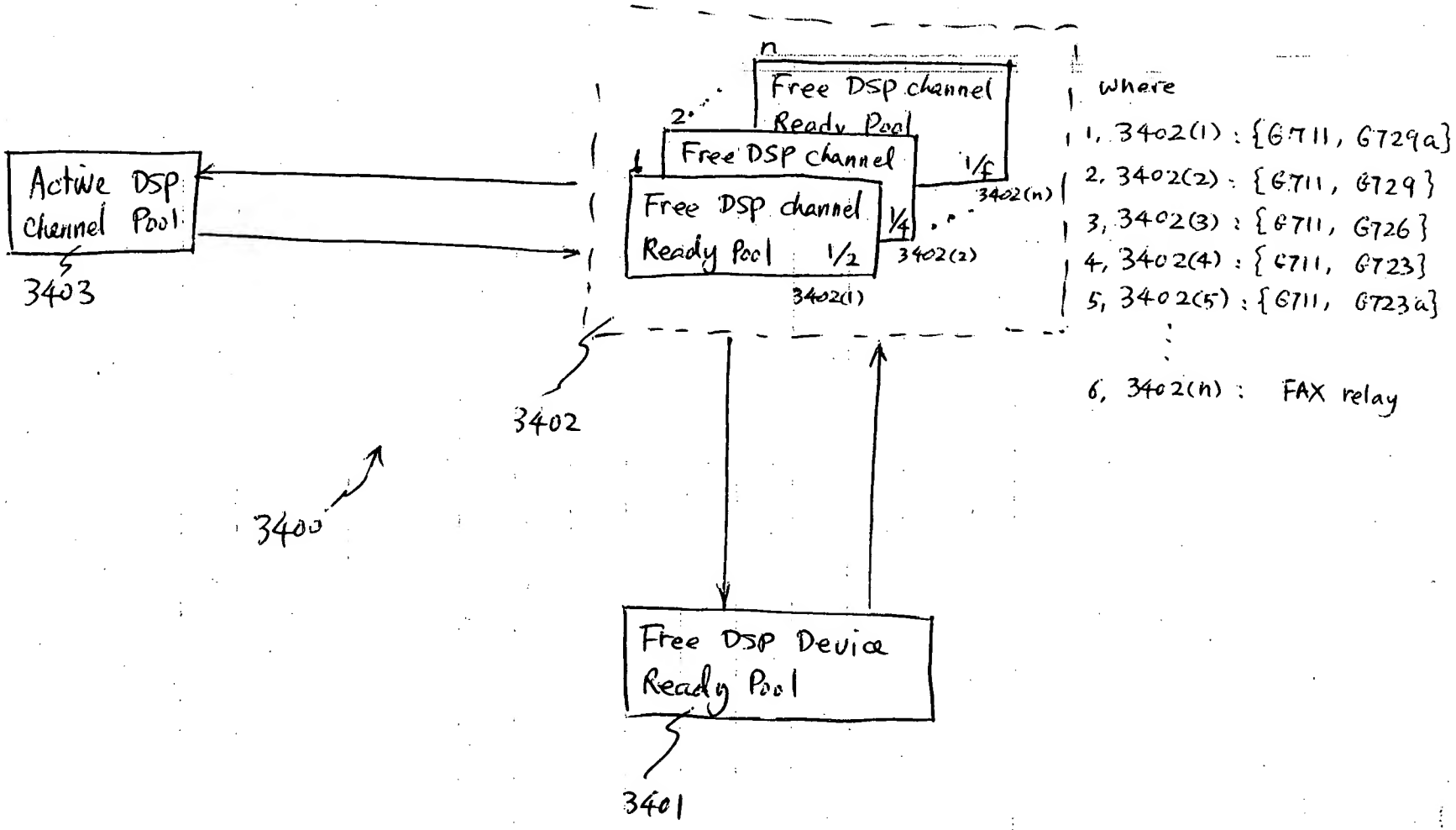

n
2
1
Free DSP channel Ready Pool
Free DSP channel
Free DSP channel Ready Pool 1/2
1/4
1/f
3402(n)
3402(2)
3402(1)
Active DSP channel Pool
3403
3402
3400
Free DSP Device Ready Pool
3401
where
1, 3402(1) : {G711, G729a}
2, 3402(2) : {G711, G729}
3, 3402(3) : {G711, G726}
4, 3402(4) : {G711, G723}
5, 3402(5) : {G711, G723a}
6, 3402(n) : FAX relay

Figure 34

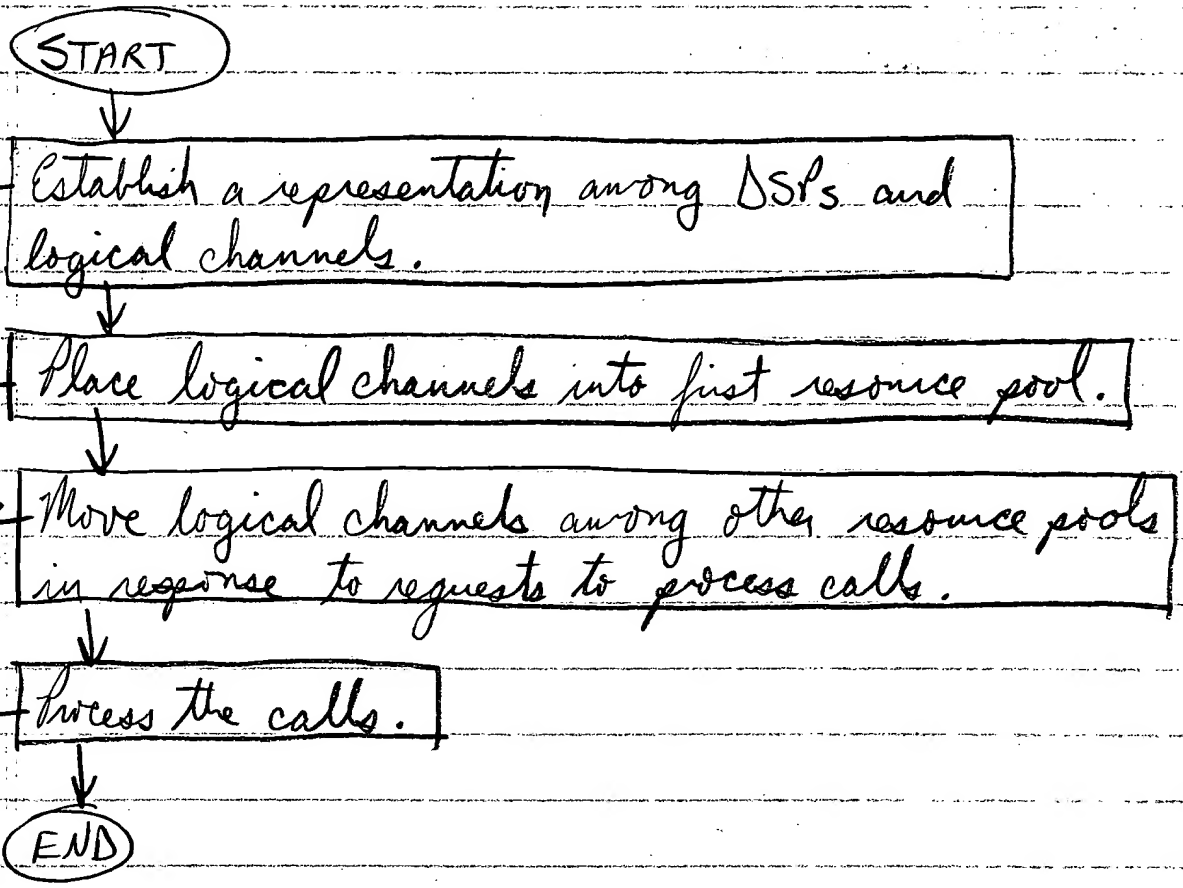

START
3502
Establish a representation among DSPs and logical channels.
3504
Place logical channels into first resource pool.
3506
Move logical channels among other resource pools in response to requests to process calls.
3508
Process the calls.
END

FIGURE 35

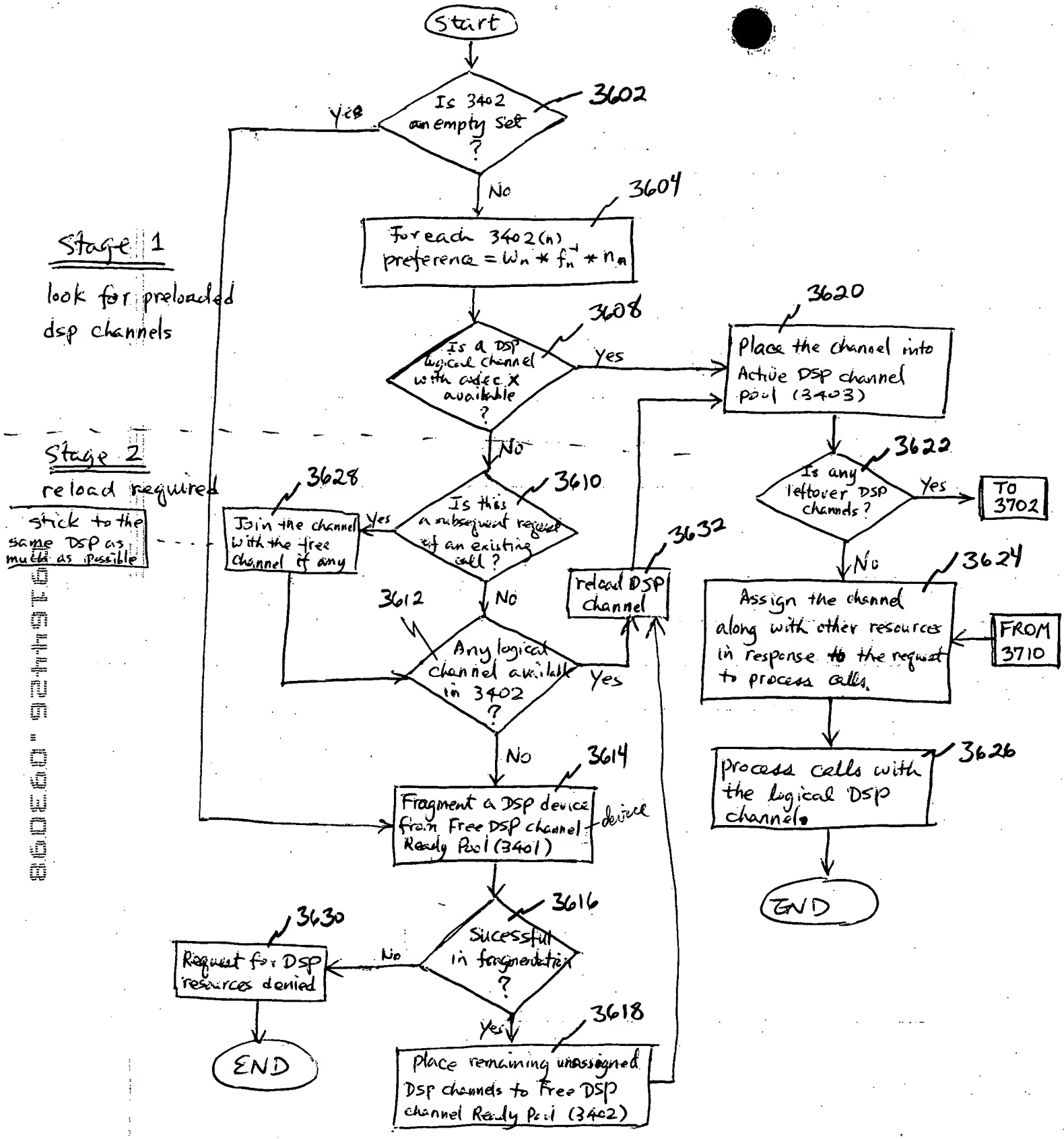

Start
Is 3402 an empty set ?
3602
Yes
No
3604
For each 3402(n) preference = $w_n * f_n^{-1} * n_n$
Stage 1
look for preloaded dsp channels
3608
Is a DSP logical channel with codec X available ?
Yes
3620
Place the channel into Active DSP channel pool (3403)
No
3622
Is any leftover DSP channels ?
Yes
TO 3702
No
3624
Assign the channel along with other resources in response to the request to process calls.
FROM 3710
3626
process calls with the logical DSP channels
END
Stage 2
reload required
stick to the same DSP as much as possible
3628
Join the channel with the free channel if any
Yes
3610
Is this a subsequent request of an existing call ?
3632
reload DSP channel
3612
No
Any logical channel available in 3402 ?
Yes
No
3614
Fragment a DSP device from Free DSP channel Ready Pool (3401)
device
3616
Sucessful in fragmentation ?
No
3630
Request for DSP resources denied
END
Yes
3618
place remaining unassigned DSP channels to Free DSP channel Ready Pool (3402)

FIGURE 36

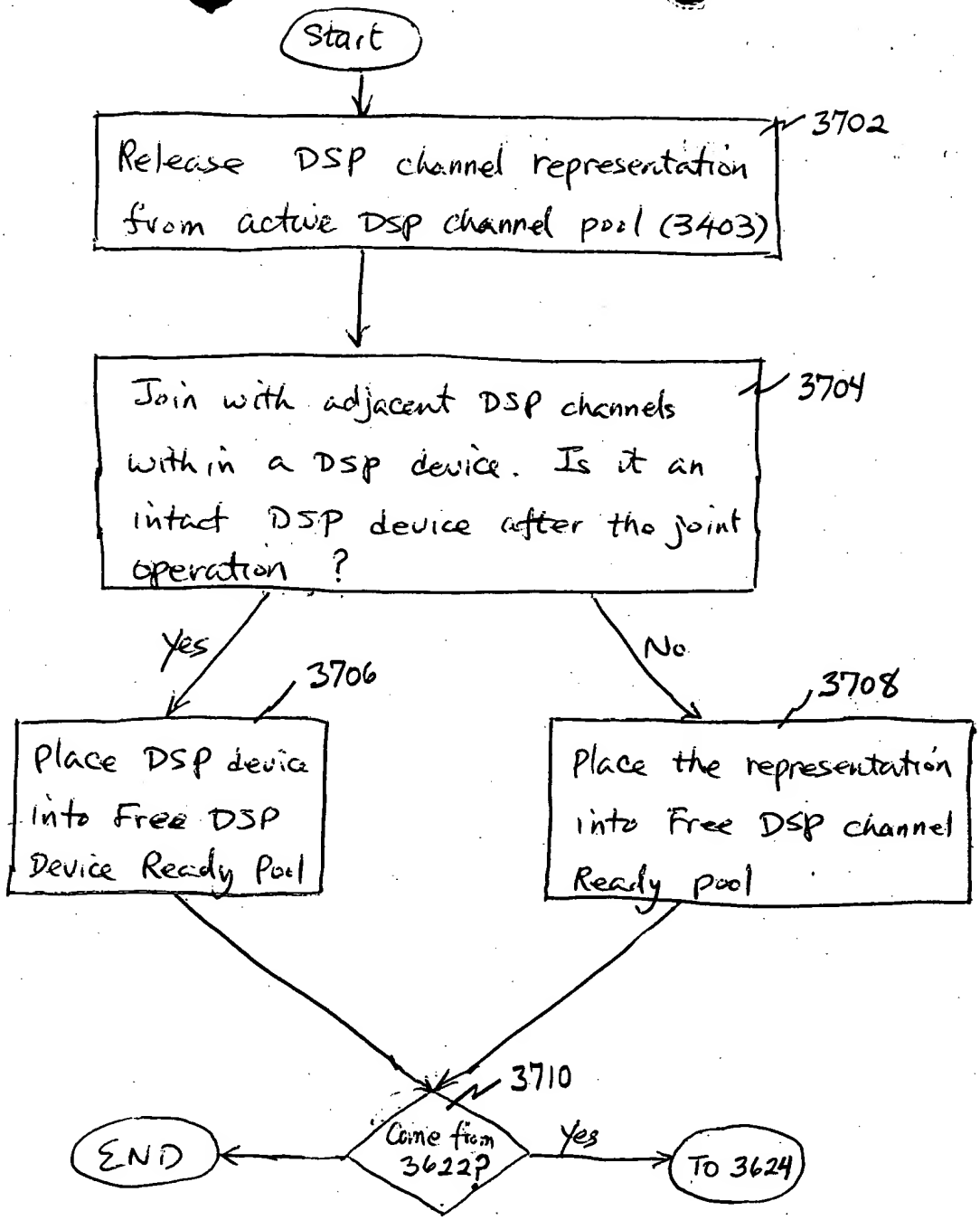

Start
Release DSP channel representation from active DSP channel pool (3403)
3702
Join with adjacent DSP channels within a DSP device. Is it an intact DSP device after the joint operation ?
3704
Yes
No
3706
Place DSP device into Free DSP Device Ready Pool
3708
Place the representation into Free DSP channel Ready pool
3710
Come from 3622?
Yes
END
To 3624

FIGURE 37

860E60 92nd ST 60

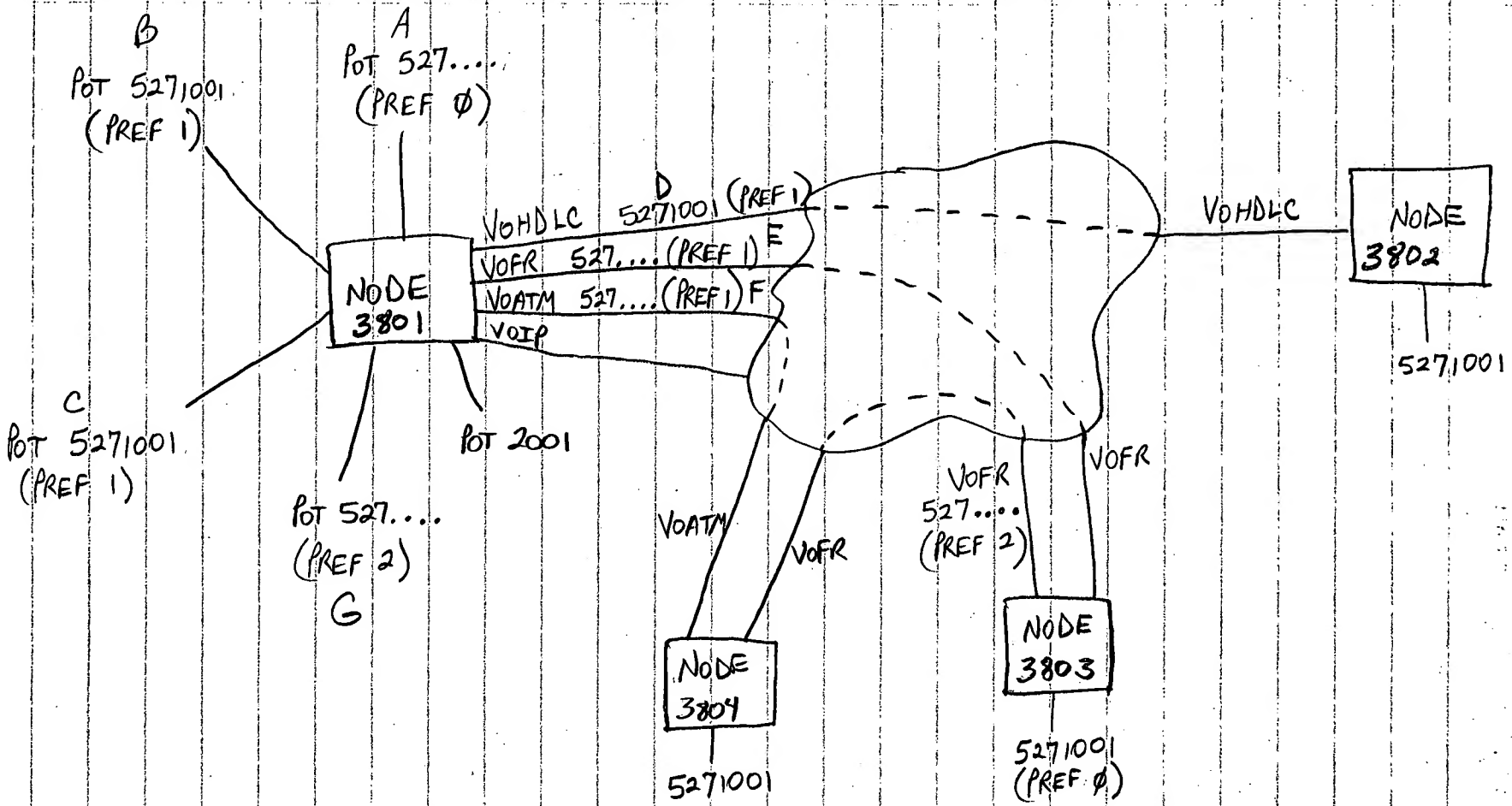


FIGURE 38

PRIORITY		
1	POT 527.... (PREF ∅)	A
2	POT 527 1001 (PREF 1)	B
3	POT 5271001 (PREF 1)	C
4	VOHDLC 5271001 (PREF 1)	D
5	VOFR 527.... (PREF 1)	E
6	VOATM 527.... (PREF 1)	F
7	POT 527.... (PREF 2)	G

FIGURE 39

860660 "92m9760

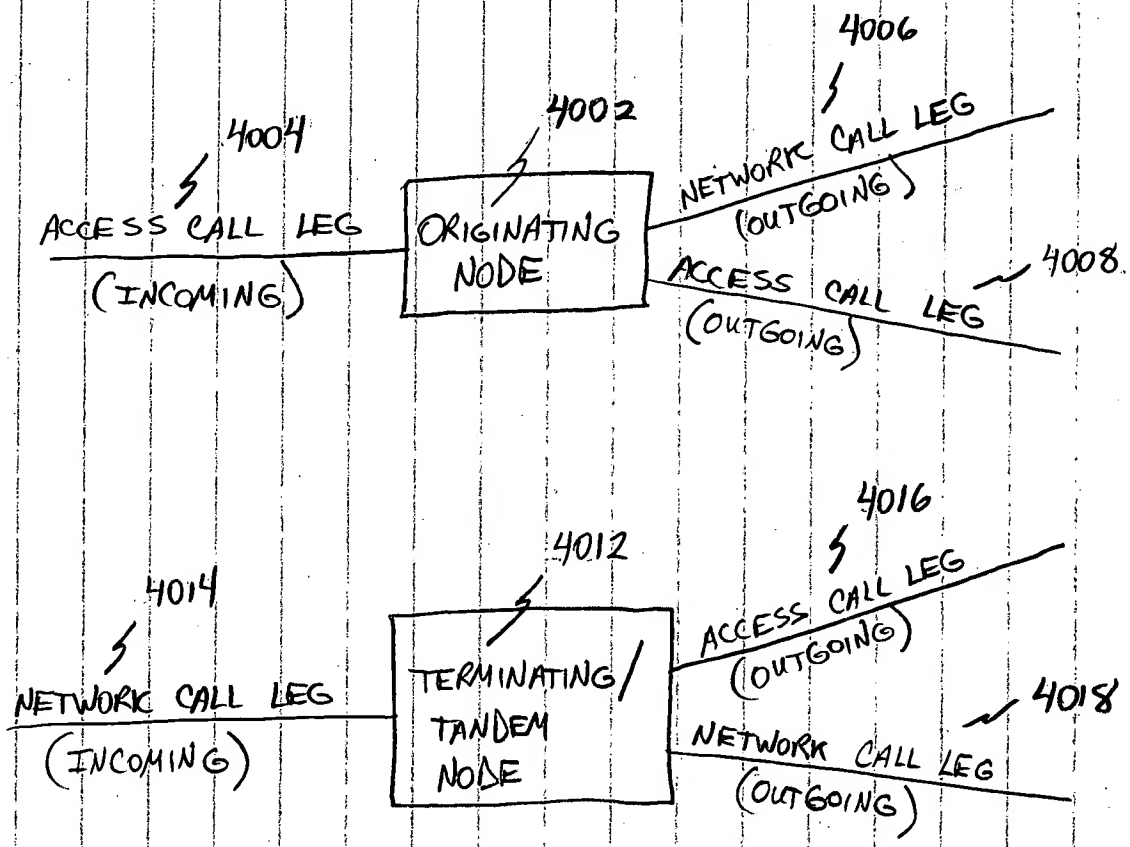


FIGURE 40

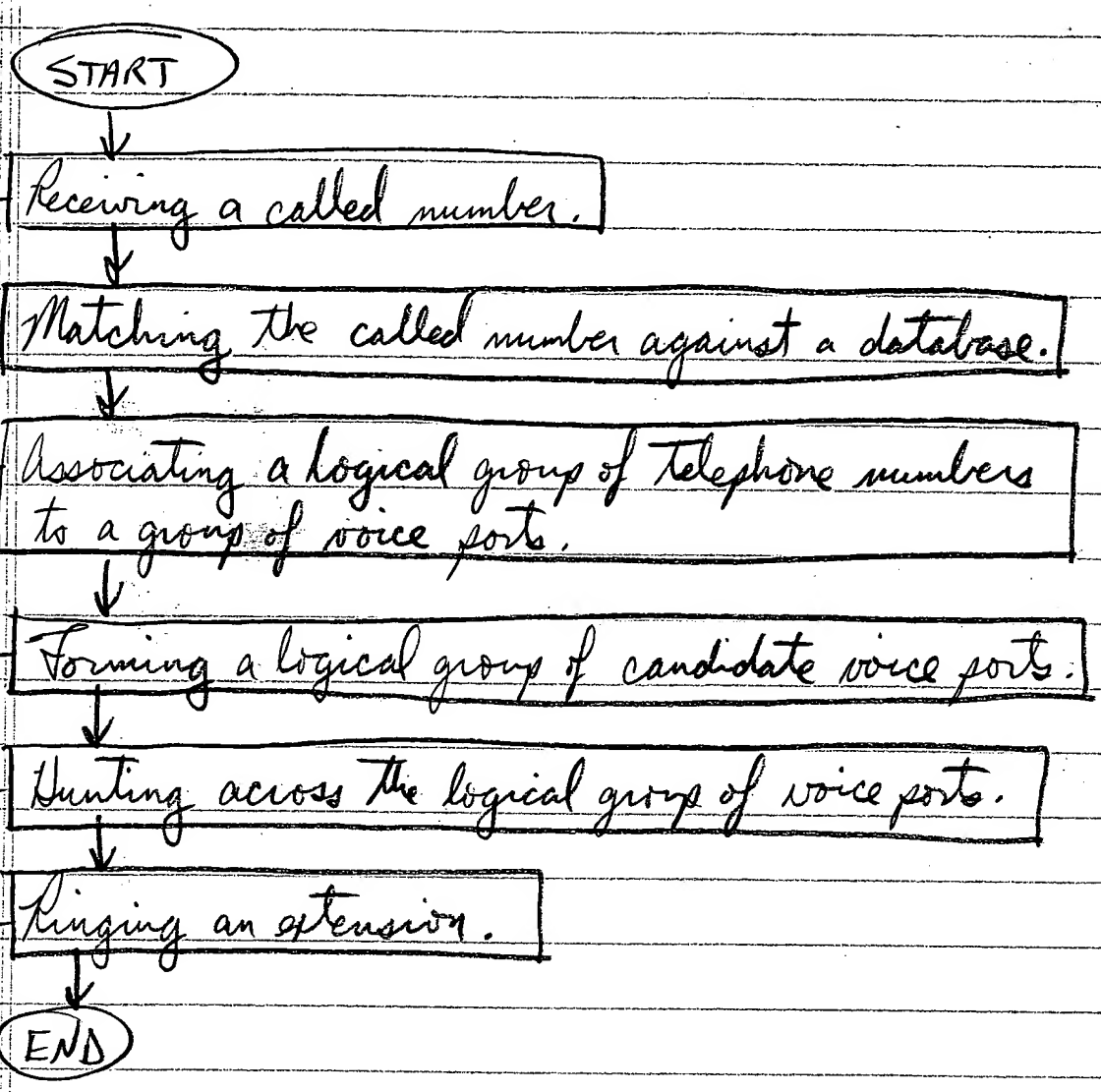

START
4102
Receiving a called number.
4104
Matching the called number against a database.
4106
Associating a logical group of telephone numbers to a group of voice ports.
4108
Forming a logical group of candidate voice ports.
4110
Hunting across the logical group of voice ports.
4112
Ringing an extension.
END

FIGURE 41

860E60" 92th9T60

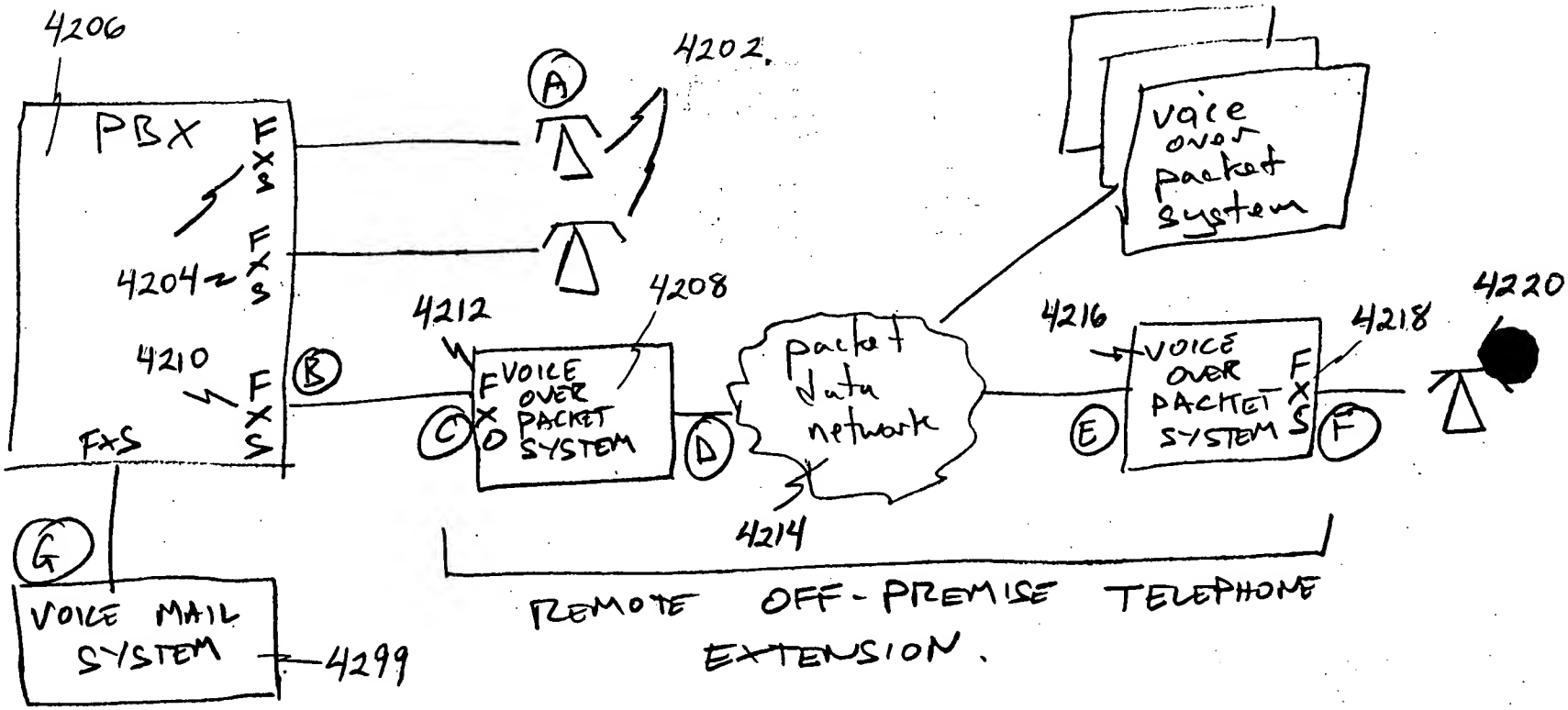


FIGURE 42

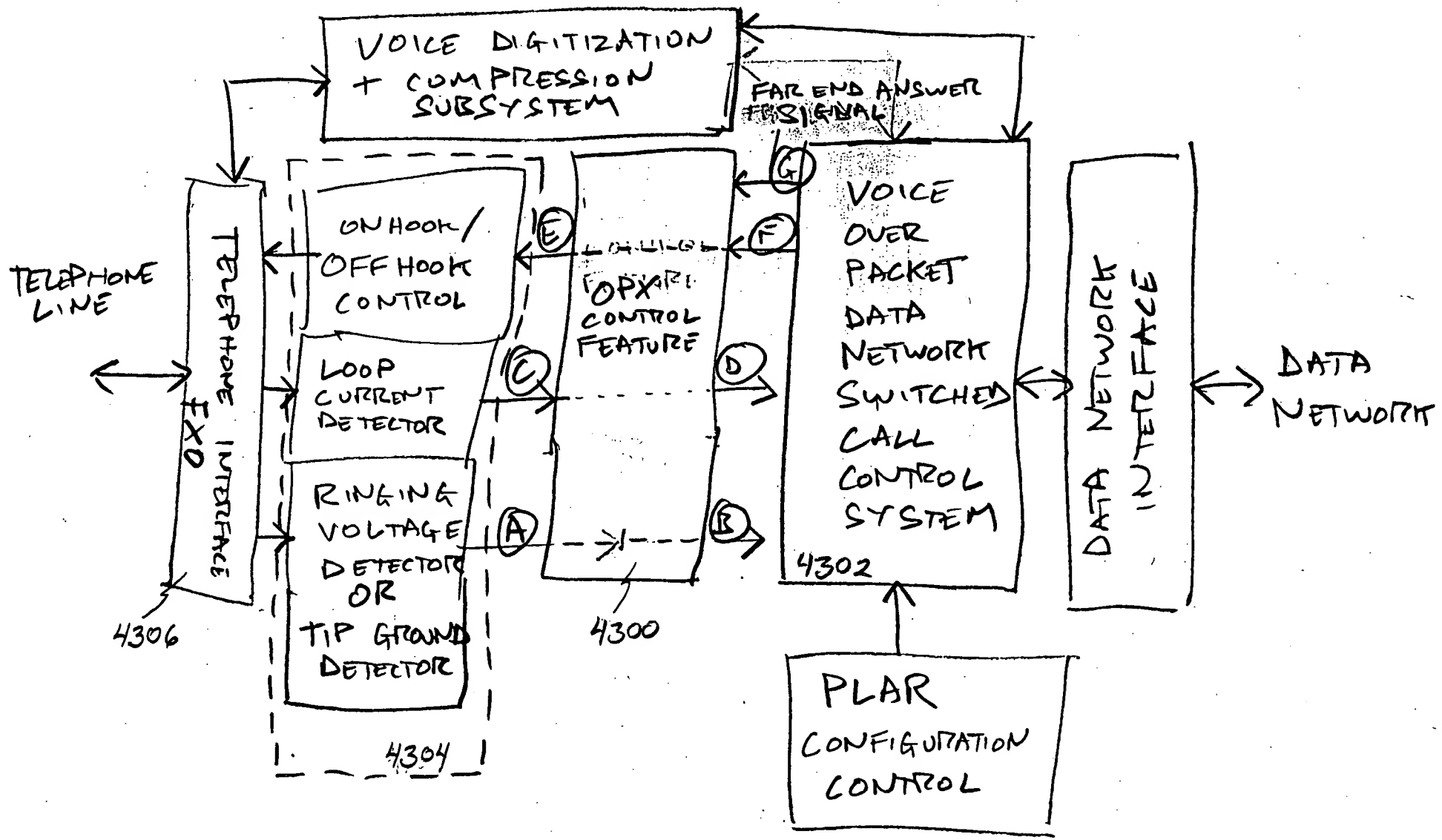

VOICE DIGITIZATION + COMPRESSION SUBSYSTEM
FAR END ANSWER SIGNAL
TELEPHONE LINE
TELEPHONE INTERFACE
FXO
ON HOOK / OFF HOOK CONTROL
LOOP CURRENT DETECTOR
RINGING VOLTAGE DETECTOR OR TIP GROUND DETECTOR
OPX CONTROL FEATURE
VOICE OVER PACKET DATA NETWORK SWITCHED CALL CONTROL SYSTEM
DATA NETWORK INTERFACE
DATA NETWORK
PLAR CONFIGURATION CONTROL
A
B
C
D
E
F
G
4306
4304
4300
4302

FIGURE 43

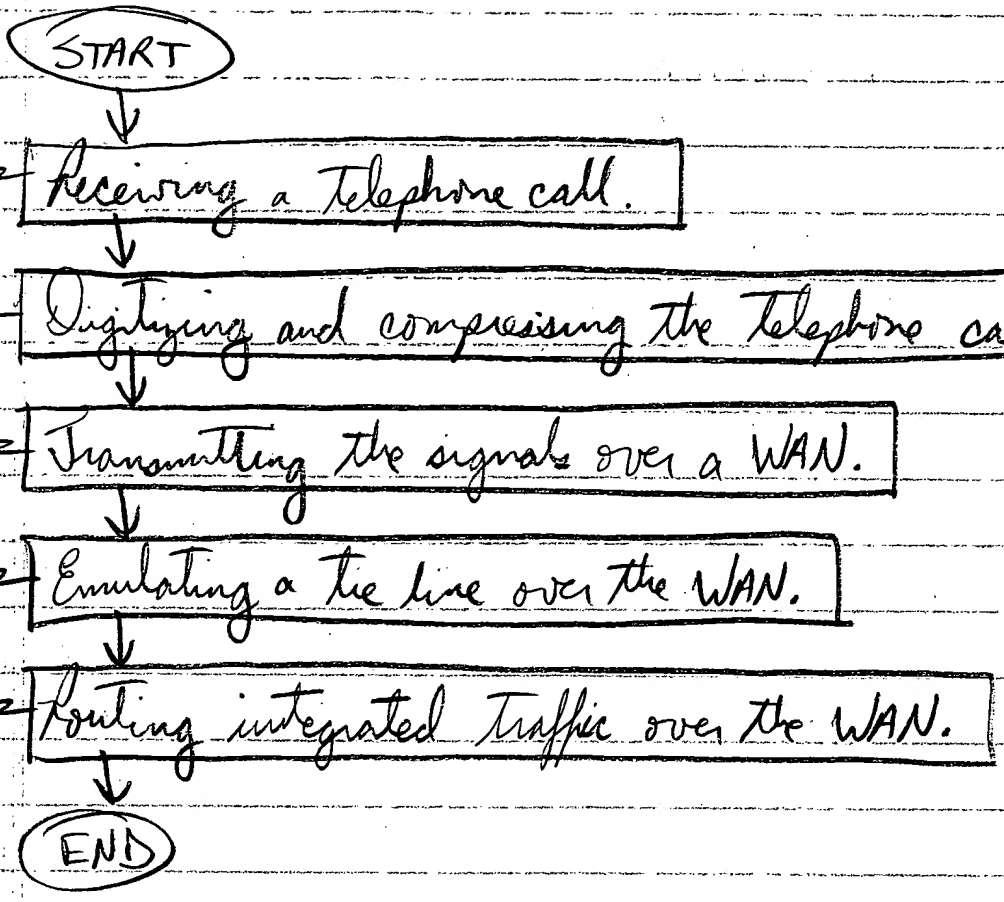

START
4402
Receiving a Telephone call.
4404
Digitizing and compressing the Telephone call signals.
4406
Transmitting the signals over a WAN.
4408
Emulating a tie line over the WAN.
4410
Routing integrated Traffic over the WAN.
END

FIGURE 44

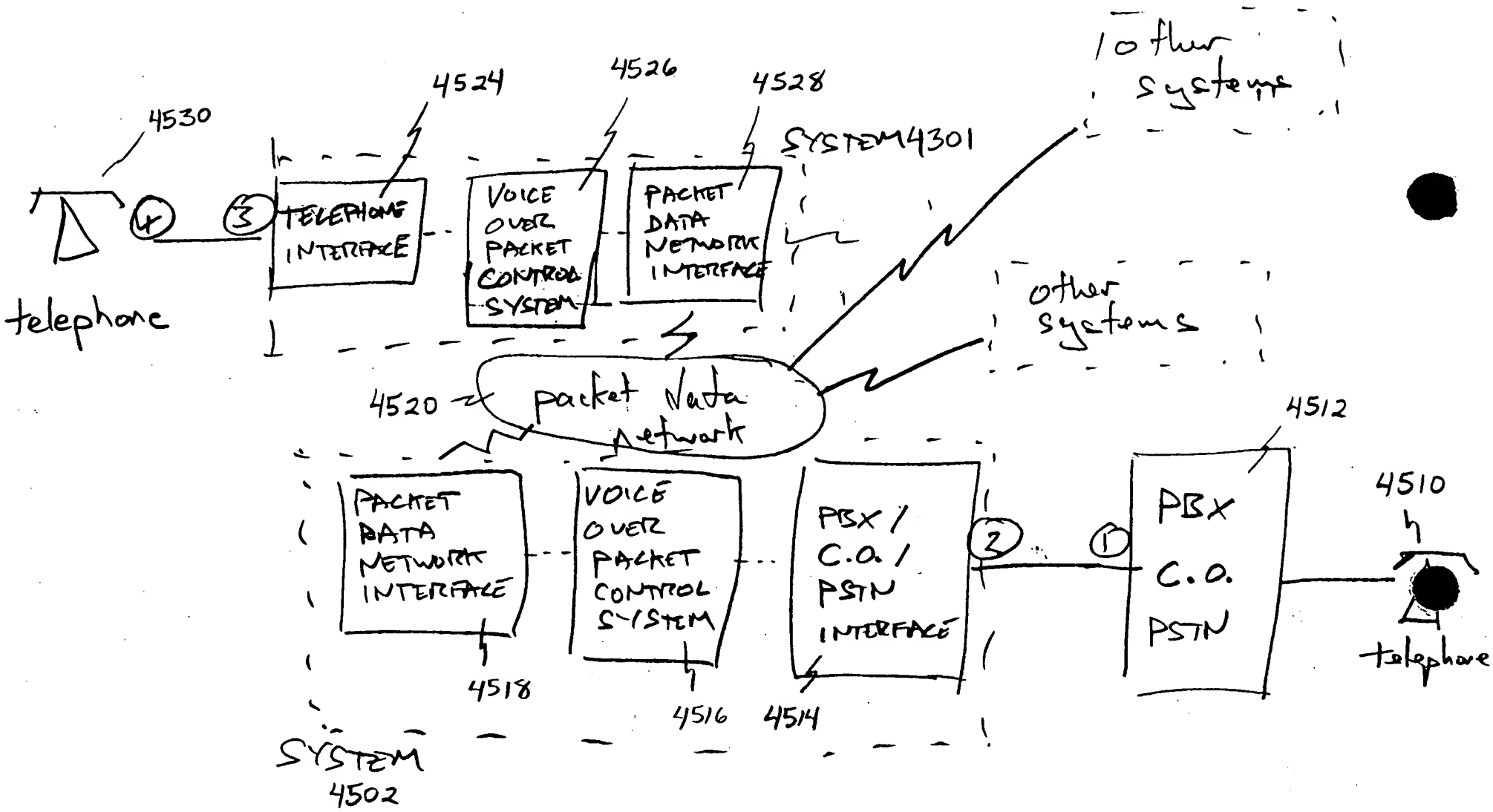

4530
4524
4526
4528
other systems
SYSTEM 4301
telephone
4
3
TELEPHONE INTERFACE
VOICE OVER PACKET CONTROL SYSTEM
PACKET DATA NETWORK INTERFACE
other systems
4520
packet data network
4512
PACKET DATA NETWORK INTERFACE
VOICE OVER PACKET CONTROL SYSTEM
PBX / C.O. / PSTN INTERFACE
2
1
PBX
C.O.
PSTN
4510
telephone
4518
4516
4514
SYSTEM 4502

FIGURE 45

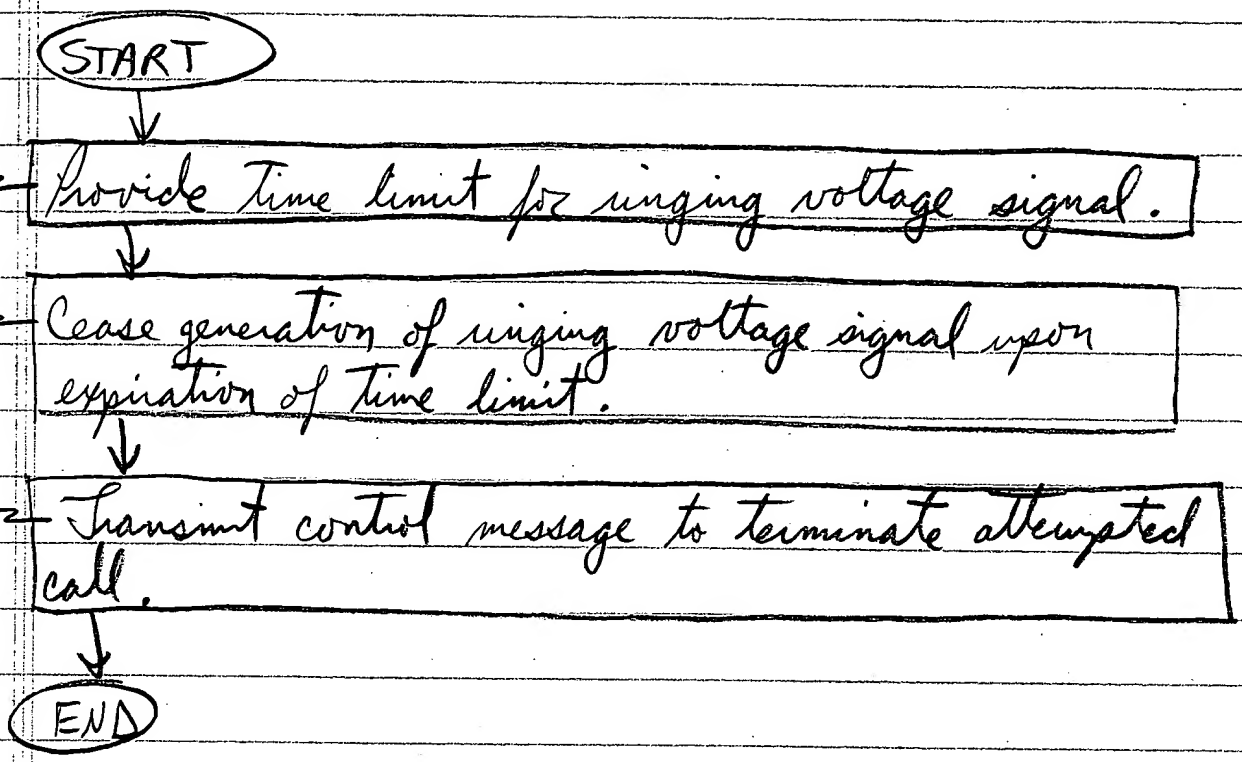

START
4602
Provide time limit for ringing voltage signal.
4604
Cease generation of ringing voltage signal upon expiration of time limit.
4608
Transmit control message to terminate attempted call.
END

FIGURE 46